

IEEE Design&Test

Call for Papers for a Special Issue on Silicon Lifecycle Management (SLM)

Aim and Scope

With increasing system complexity, security, stringent runtime requirements for functional safety, and cost constraints of a mass market, the reliable and secure operation of electronics in safety-critical, enterprise servers and cloud computing domains are still a major challenge. While traditionally design time and test time solutions were supposed to guarantee the in-field dependability and security of electronic systems, due to complex interaction of runtime effects from running workload and environment, there is a great need for a holistic approach for silicon lifecycle management, spanning from design time to in-field monitoring and adaptation. Therefore, the solutions for lifecycle management should include various sensors and monitors embedded in different levels of the design stack, access mechanisms and standards for such on-chip and in-system sensor network, as well as data analytics on the edge and in the cloud. This is a very timely topic for both industry and academia, and spans in various parts of the silicon ecosystem from technology, foundry, design, EDA, test solutions, verification and debug, to in-field deployment, as well as IP, SoC and system integration, EDA, and cloud sectors. It also needs the use of data analytics at chip, system and cloud as well as the standards and interaction of various DfX infrastructures.

Topics of Interest

This special issue is dedicated to various aspect of Silicon Lifecycle Management. It aims to cover diverse aspects of this topic from design, EDA, on-chip infrastructure for test, debug, reliability, and security as well as data analytics. The specific topics of interest include but are not limited to:

- Design and placement of various sensors and monitors for functional safety and security
- Standards for sensor data aggregation
- Data analytics for sensor data processing
- Anomaly detection for security and functional safety
- Machine learning for in-field system health monitoring
- Multi-layer dependability evaluation
- In-field verification and validation
- Fault tolerance and self-checking circuits
- Aging effects on electronics
- Power-up, power-down and periodic tests
- In-field configuration and adaptation
- Reuse and extension of test, debug and repair infrastructure for in-filed management
- System level test
- Preventive Maintenance
- Functional and structural test generation
- Graceful degradation
- Useful remaining lifetime prediction
- Failure prediction and forecasting
- Attack prediction and prevention
- Cross-layer solutions

Submission Guidelines

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at <https://mc.manuscriptcentral.com/dandt>. Indicate that you are submitting your article to the “*Special Issue on Silicon Lifecycle Management (SLM)*”. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (30 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Information at: <https://iee- ceda.org/publication/ieee-design-test-dt/author-info>.

Schedule

- Open for submissions : August 1, 2022
- Submission deadline : November 15, 2022
- Notification First Round : January 31, 2023
- Revision submission : March 31, 2023
- Final decisions : May 15, 2023
- Tentative publication : Fall 2023

Guest Editors

- **Mehdi Tahoori**, Karlsruhe Institute of Technology, Germany
- **Yervant Zorian**, Synopsys Inc., USA

For questions and further information, please contact the lead guest editor at: mehdi.tahoori@kit.edu