



### ACM Transactions on Design Automation of Electronic Systems

*Special Issue on High-Level Synthesis for FPGA: Next-Generation Technologies and Applications*

#### Guest Editors:

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Due to the end of Dennard scaling and Moore's law, complex hyper-pipelined processors are increasingly replaced by heterogeneous System-on-Chip (SoC) architectures with many specialized components. FPGA devices are becoming common targets for these systems since they allow fast turn-around time, field upgradability, and easy deployment of hardware/software solutions. To cope with the increasing complexity of such systems, designers need to raise the abstraction level from custom design flows to high-level approaches. High-level synthesis (HLS) is a popular method that allows designers to describe the functionality of a component at the software level and automatically generate the corresponding hardware description, reducing the gap between application and hardware designers. Since HLS has been making a great amount of progress and an increasing number of different application domains are pushing designers towards hardware acceleration, HLS is becoming a key enabling technology for FPGA design.

The application landscape for hardware acceleration is rapidly and deeply changing. Modern applications are increasingly based on machine learning that require access to huge amounts of data to extract valuable knowledge and make accurate predictions. Also, novel technologies like quantum computing are opening novel research questions on how to design accelerators for these systems (including post-quantum cryptography). The combined requirements of modern technologies and applications pose novel challenges and threats for high-level synthesis. For example, side-channel and adversarial attacks are serious threats for security and machine learning applications.

#### Topics

This special issue aims at presenting the latest advances in high-level synthesis for FPGAs, focusing on the interplay with (and between) artificial intelligence and security. Topics of interest include, but are not limited to, the following:

- Use of high-level synthesis for emerging applications (e.g., AI, post-quantum cryptography)
- Use of emerging methods for high-level synthesis (e.g., machine learning for design space exploration and predictions)
- Domain-specific languages and compiler-based optimizations to specify and integrate extra-functional properties (e.g., security requirements) during high-level synthesis
- Algorithms for scheduling, binding, and controller synthesis for the co-optimization of hardware security protections
- Automatic synthesis (and protection) of near-memory computation systems
- Identification of security vulnerabilities in HLS-generated designs

#### Important Dates

- Submissions deadline: 30 June 2021
- First-round review decisions: 31 August 2021
- Deadline for revision submissions: 15 October 2021
- Notification of final decisions: 31 November 2021
- Tentative publication: January/February 2022

### **Submission Information**

Authors are encouraged to submit high-quality original research contributions that will not require major revisions. Please identify clearly the additional material from any original conference paper in your submitted manuscript. Submissions of relevant original work not previously presented at any conference are especially welcome. Concurrent submission to any other conference or journal is a ground for rejection of a manuscript without review. All papers will be fully refereed to the usual journal standards. Submissions should be made through the ACM TODAES submission site (<http://mc.manuscriptcentral.com/todaes>) and formatted according to TODAES author guidelines at: <https://dl.acm.org/journal/todaes/author-guidelines>.

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