IEEE Design&Test

Call for Papers

Special Issue on Machine Learning for CAD / EDA

Aims and Scope

Moore's Law is still alive and well, as far as increasing the complexity of ICs is concerned. Logic ICs with about 20 billion transistors or even more are being manufactured today. Their design, verification and test are daunting tasks. At the same time that complexity keeps increasing relentlessly, novel technical challenges (e.g. mask patterning challenges, increasing manufacturing variations) appear as we are moving ever closer to the limits of technology scaling.

Machine learning (ML), including AI techniques, is increasingly being researched as a potential solution to the "design crisis" resulting from these developments. It is being applied for IC design throughout the entire design flow, from system level optimization all the way down to layout optimization and mask preparation.

This special issue seeks original submission on ML applications to the entire design flow – including ML applications to validation and test. The application of machine learning to mask preparation and layout generation are topics which are seeing very active research recently. ML is also being applied to improve the robustness of integrated circuits and systems. Power and thermal management are probably the most important limiting factors for ICs today - ML-based techniques are being explored to address this bottleneck. All these topics, as well as further potential topics mentioned below, are of interest to this special issue.

In addition to submissions from academia, submissions from industry are much welcome.

Topics of Interest include, but are not restricted to:

- ML for system-level design
- ML approaches to logic design and synthesis
- ML for timing
- ML for clock networks and power grids
- ML for variation-aware design, analysis and optimization
- ML for physical design
- ML for analog design
- ML for power and thermal management
- ML for Design Technology Co-Optimization (DTCO)
- ML methods to predict aging and reliability

- Labeled and unlabeled data in ML for CAD
- ML techniques for resource management in many cores
- ML for verification and validation
- ML for test
- ML for library design and optimization

Submission Guidelines:

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt. Indicate that you are submitting your article to the special issue on Machine Learning for CAD / EDA. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Resources at: http://www.ieee.org/publications_standards/publications/authors/magazines.html to view links in Submission Guidelines Basics and Electronic Submission Guidelines and requirements.

Schedule:

• Submission Deadline: 15 January 2021
• Review Notification: 28 February 2021
• Revisions due: 30 March 2021
• Final Notification: 30 April 2021
• Final Papers Due: 15 May 2021

Guest Editors

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