Proudly sponsor the 24th annual
IEEE Electronic Design Process Symposium
Accelerating Design and Manufacturing

September 21 & 22, 2017
SEMI, 673 S. Milpitas Blvd, Milpitas, CA 95035

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IEEE EDPS 2017 Program focuses on acceleration methods for the design and manufacturing processes. The event will be held at the SEMI facility and provide a forum for EDA, foundry and design industries to address the design and the manufacturing issues. Emerging trends like machine learning and big data analysis and their impact on the above-mentioned issues will be addressed. The full two day program features prominent speakers from industry and academia in multiple domains.

Design Acceleration	Driving to Higher Yield
Rajesh Gupta, John Lee, CP Hung and Bill Bottoms	Keith Arnold, Asim Salim, Gerard John, Juan Rey
Accelerating Debug & Validation	**Machine Learning**
Gajinder Panesar, Eduardo Bolanos, Al Czamara, Vikas Kumar	Paul Franzon, David White, Rob Aitken, Jeff Dyke, Abhijit Chatterjee

We will conclude with a panel discussion to analyze new directions for accelerating design and manufacturing processes.

Keynote Speakers

Antun Domic
CTO, Synopsys
Exploit close relationship of design & manufacturing to accelerate product intro

Zoe Conroy
Sr. Manager, Cisco
Using System level testing as a conduit to HVM

Jim Hogan
Private Investor
EDA industry's participation in cognitive age: The fourth industrial revolution

Pankaj Mehra
VP, Western Digital
Getting EDA ready for the data centric architecture

A complete schedule is available at ieee-edps.org. Early registration and discounted rates will close on August 31. To register, please go to edps2017.eventbrite.com.

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