IEEE Design&Test

Call for Papers

Special Issue on Benchmarking Machine Learning Systems and Applications

Aims and Scope:

Machine learning (ML) has been proven to play a key role in the design of next generation systems and is now being deployed in a plethora of applications and systems, across industry-segments. The popularity gained by ML with its superior performance, has not only led to its broad applicability in a wide range of applications, but has also increased the functional design and test requirements of the system. To reap higher yield from the ML applications and systems, real-time performance, power and system efficiency are key. Given the rapid advances, across industry and academia in this direction, benchmarking these ML applications and systems is critical. Such benchmarking will also help the community to analyze and compare the solutions in a fair manner.

In this special issue, we put primary focus on metrics, and methods to assess ML, and more so on test chips and systems. We anticipate real industry perspectives in this special issue, capturing latest advances and research requirements in this direction. Secondly, we intend to bring together cross-layer aspects relating to deployment of ML on systems, architectural considerations, and design methodologies for a truly efficient deployment. In addition to ML-specific research for accelerator design, challenges relating to the co-existence of ML and non-ML hardware, robust ML architectures for different scales (IoT, embedded system and data centers) are of additional interest.

Topics of Interest Include but not restricted to

The special issue is looking for innovative research that focuses on design of accelerators for machine learning applications and architectures deployed in different systems and IoT devices. The topics of interest for this special issue includes but not limited to the following topics:

- Benchmarking metrics, and methods to assess ML
- Cross-layer metrics and assessment of efficient deployment of ML systems
- Benchmarking on test chips, real industry perspectives
- ML & DL techniques for enabling hardware design

- ML accelerators with approximate computing units
- ML model compression and acceleration for hardware
- Reconfigurable accelerator architectures for ML
- ML accelerators for high performance computing and data centers
- Neuromorphic architectures for ML
- HW/SW co-design in a system with ML and non-ML hardware
- Architectures that resist ML adversaries

Submission Guidelines:

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt. Indicate that you are submitting your article to the Special Issue on *Near-Memory and In-Memory Processing*. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Resources at http://www.ieee.org/publications_standards/publications/authors/magazines.html to view links in Submission Guidelines Basics and Electronic Submission Guidelines and requirements.

Schedule:

- Article due for review: September 1, 2020
- Reviews completed: November 1, 2020
- Article revisions due: December 15, 2020
- Notice of final acceptance: January 31, 2021
- All materials due to edit: February 28, 2021
- Tentative Publication date: April 2021

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