IEEE Design&Test

Call for Papers

Special Issue on Near-Memory and In-Memory Processing

Aims and Scope:

The rapid explosion in data-intensive applications is posing unprecedented demand for superior data processing capabilities. With the end of Dennard scaling, the benefits of conventional approaches of moving stored data to processing cores and enhancing the computing capability of these cores through technology scaling have diminished. At the same time, advancements in new material and integration technologies have made the old concept of coupling compute units to memory more viable.

Near memory processing (NMP) and in-memory processing (IMP), in general, cover a wide spectrum of computing capabilities embedded in close proximity to and/or inside the memory array. NMP/IMP approaches can reduce the latency and energy consumption associated with data movement throughout the cache and memory hierarchy. Moreover, NMP/IMP approaches can operate in parallel with CPU/GPU cores and other accelerators. Due to their potential to greatly reduce energy and improve execution time by reducing data movement, various NMP/IMP approaches have received substantial interest in both industry and academia.

In this context, this special issue on *Near-Memory and In-Memory Processing* will introduce, explore, and investigate challenges and opportunities in developing innovative NMP/IMP computer architectures based on conventional and emerging technologies for a wide variety of modern applications. The aim of this special issue is to offer the readers a clear perspective of the rich landscape of both academic and industrial endeavors in architecting, designing and testing NMP/IMP architectures and systems. The special issue will not only showcase the state-of-the-art but also articulate the innovations and advances required for widespread adoption of such systems in existing and emerging application domains.

In particular, the special issue will cover both hardware-, software- and algorithm-level techniques that enable and advance near-memory and in-memory processing systems (see topics of interest). It will include innovative design of circuit components, processor micro-architecture, heterogeneous systems, memory interface, software support, workloads analysis, and communications. It will delve into the design automation methodologies and optimizations, programing model, compilers to support NMP/IMP, verification & testing approaches, and concerns for the system robustness and security. The special issue will also incorporate various application domains that will benefit from the NMP or IMP.

Topics of Interest Include but not restricted to

Any research and practice issues related to and within the context of near- and in-memory processing, including the following:

- Near- or in-memory data management and processing models
- Circuit and architecture techniques for near- or in-memory processing
- Memory and storage technologies for near- or in-memory processing, conventional & emerging
- Heterogeneous and parallel systems incorporating near- or in-memory processing
- System/architecture interaction, execution model, interfaces for near- or in-memory computing
- Energy management issues in near- or in- memory processing
- Programming models and compilation for near- or in-memory processing
- System software support for near- or in-memory processing
- Hardware security, energy efficiency, fault tolerance, performance issues
- Workloads analysis and benchmarking for near- or in-memory processing
- Adoption issues of near- or in-memory processing and solutions
- Specialized architectures for key workloads (ML, AI, genomics, databases, graph processing, etc.) taking advantage of near- or in-memory processing

Submission Guidelines:

Prospective authors should follow the submission guidelines for IEEE Design & Test. All manuscripts must be submitted electronically to IEEE Manuscript Central at https://mc.manuscriptcentral.com/dandt. Indicate that you are submitting your article to the Special Issue on *Near-Memory and In-Memory Processing*. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere. Manuscripts must not exceed 5,000 words, including figures (with each average-size figure counting as 200 words) and a maximum of 12 references (50 for surveys). This amounts to about 4,000 words of text and a maximum of five small to medium figures. Accepted articles will be edited for clarity, structure, conciseness, grammar, passive to active voice, logical organization, readability, and adherence to style. Please see IEEE Design & Test Author Resources at http://www.ieee.org/publications_standards/publications/authors/magazines.html to view links in Submission Guidelines Basics and Electronic Submission Guidelines and requirements.

Schedule:

- Article due for review: June 15, 2020
- Reviews completed: August 31, 2020
- Article revisions due: September 30, 2020
- Notice of final acceptance: October 31, 2020
- All materials due to edit: November 15, 2020
- Publication date: January 2021

Guest Editors

Hai “Helen” Li, Duke University (USA) hai.li@duke.edu
Alaa R. Alameldeen, Intel Corp. (USA) alaa.r.alameldeen@intel.com
Onur Mutlu, ETH Zürich (Switzerland) onur.mutlu@inf.ethz.ch