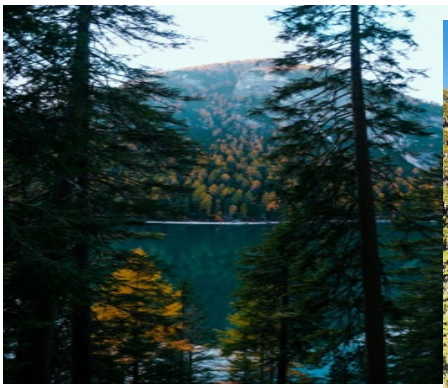

# 40th IEEE International Conference on Computer Design

## ICCD 2022

October 23 – 26, 2022
Lake Tahoe, USA

https://www.iccd-conf.com

## Call for Paper

ICCD encompasses a wide range of topics in the research, design, and implementation of computer systems and their components. ICCD's multi-disciplinary emphasis provides an ideal environment for developers and researchers to discuss practical and theoretical work covering systems and applications, computer architecture, verification and test, design tools and methodologies, circuit design, and technology.

## Theme

The theme for ICCD'22 is
**Hardware Architecture for AI and Machine Learning**

We solicit submissions on this theme for any of the ICCD tracks.

## Tracks

Manuscripts describing original work on one of the following tracks are welcome.

**Track 1. Computer Systems:** System architecture and software (compiler, programming language/model, firmware, OS, hypervisor, runtime) design and co-design for embedded/real-time systems; System support and compilers for multi/many cores, co-processors, and accelerators; System support for security, reliability, and energy efficiency and proportionality; Virtual memory; System support for emerging technologies, including NVM, quantum, neuromorphic, bio-inspired computing, machine learning and artificial intelligence applications; Specialized OS, runtime, and storage systems for data center and cloud/edge computing, high-performance computing (HPC), exascale system, and serverless computing.

Track Chairs: *Clayton Hughes (Sandia National Laboratories); Hung-Wei Tseng (University of California at Riverside)*

**Track 2. Processor Architecture:** Microarchitecture design techniques for single-threaded and multi/many-core processors, such as instruction-level parallelism, pipelining, caches, branch prediction, multithreading, and networks-on-chip; Techniques for low-power, secure, and reliable processor architectures; Hardware acceleration for emerging applications including NVM, quantum, neuromorphic, bio-inspired; Hardware support for processor virtualization; Real-life design challenges: case studies, tradeoffs, retrospectives.

Track Chairs: *Khaled Khasawneh (George Mason University); Rui Hou (Chinese Academy of Sciences)*

**Track 3. Test, Verification and Security:** Design error debug and diagnosis; Fault modeling; Fault simulation and ATPG; Analog/RF testing; Statistical test methods; Large volume yield analysis and learning; Fault tolerance; DFT and BIST; Functional, transaction-level, RTL, and gate-level modeling and verification of hardware designs; Equivalence checking, property checking, and theorem proving; Constrained-random test generation; High-level design and SoC validation; Hardware security primitives and methodologies; Side-channel analysis, attacks and mitigations for processors and accelerators; Interaction between test, security and trust.

Track Chairs: *Rujia Wang (Illionois Institute of Technology); Sumit Jha (University of Texas at San Antonio)*

**Track 4. Electronic Design Automation:** System-level design and synthesis; High-level, logic and physical synthesis; Analysis and optimization of timing, power, variability/yield, temperature, and noise; Physical design, including partitioning, floorplanning, placement, and routing; Clock-tree synthesis; Verification methods at different levels of the EDA flow; Tools for multiple-clock domains, asynchronous, and mixed-timing methodologies; CAD support for accelerators, FPGAs, SoCs, ASICs, NoC, and general-purpose processors; CAD for manufacturing, test, verification, and security; Tools and design methods for emerging technologies (photonics, MEMS, spintronics, nano, quantum); interaction of EDA and AI/ML.

Track Chairs: *Benjamin Carrion Schafer (University of Texas at Dallas); Eleonora Testa (Synopsys)*

**Track 5. Logic and Circuit Design:** Circuit design techniques for digital, memory, analog and mixed-signal systems; Circuit design techniques for high performance and low power; Circuit design techniques for robustness under process variability, electromigration, and radiation; Design techniques for emerging and maturing technologies (MEMS, nano-spintronics, quantum, flexible electronics, multi-gate devices, in-memory computing); Asynchronous circuit design; Signal-processing, graphic-processor, and datapath circuits.

Track Chairs: *Andre Reis (Universidade Federal do Rio Grande do Sul); William Hung (Cadence)*

## Organizing Committee

**General Chair**:
- Rathish Jayabharathi
  *Intel, USA*

**Program Chairs**:
- Amro Awad
  *North Carolina State University, USA*
- Christian Pilato
  *Politecnico di Milan, Italy*

**Web Chairs**:
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  *University of Connecticut, USA*
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  *University of Hawaii, USA*
- Sandip Kundu
  *Univ. of Massachusetts Amherst, USA*

## Important Dates

**Abstract Registration:**
June 4th, 2022 (11:59pm AOE)
**Full Paper Submission:**
June 11th, 2022 (11:59pm AOE)
**Notification:**
August 21st, 2022

## Paper Format & Publication

Papers must be submitted as a single PDF file following the submission guidelines that is made available at the conference website.

The proceedings will be published by IEEE. At least one author should register as a regular attendee for the paper to be included in the proceedings.

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