IEEE/ACM
2023 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN
ICCAD
42nd Edition

iccad.com

San Francisco, CA, USA
October 29 - November 2, 2023

CALL FOR PAPERS

Original technical submissions on, but not limited to, the following topics are invited:

1) System-level CAD

1.1 System Design

- System-level specification, modeling, simulation, design flaws
- System-level issues for 3D integration
- System-level design case studies and applications
- HW/SW co-design, co-simulation, co-optimization, and co-exploration, platforms for emulation and rapid prototyping
- Micro-architectural transformation
- Multi-/many-core processor, GPL and heterogeneous SoC
- Memory and storage architecture and system synthesis
- System communication architecture, Network-on-chip design
- Modeling, simulation, high-level synthesis, power/performance analysis, programming of heterogeneous computing platforms
- Application driven system design for big data
- Analysis and optimization of data centers

1.2 Embedded, Cyber-Physical (CPS), IoT Systems and Software

- AI and machine learning for embedded systems
- HW/SW co-design for embedded systems
- Compute, memory, storage, interconnect for embedded systems
- Domain-specific accelerators
- Energy/power management and energy harvesting
- Real-time software and systems
- Middleware, virtual machines, and runtime support
- Dependable, safe, secure, trustworthy embedded systems
- Embedded software: compilation, optimization, testing
- CAD for IoT, edge and fog computing
- Modeling, analysis, verification of CPS systems
- Green computing (smart grid, energy, solar panels, etc.)
- CAD for application domains including wearables, health care, autonomous systems, smart cities

1.3 Tools and Design Methods with and for Artificial Intelligence (AI)

- Compilers for deep neural networks
- Design method for learning on a chip
- Deep neural network for EDA
- Tools and design methodologies for edge AI and TinyML
- Performance analysis and modeling for AI accelerators
- Reliability analysis for neural network designs

1.4 Hardware Systems and Architectures for Artificial Intelligence (AI)

- Hardware and architecture for neural networks
- System-level design for (deep) neural computing
- Neural network acceleration including GPU and ASICs
- Safe and secure machine learning
- Hardware accelerators for Artificial Intelligence (e.g, neural network, graph processing)
- Edge AI and TinyML architecture designs
- New systems and architectures for neural networks, such as optical neural networks, chiplets

1.5 Reconfigurable Computing

- Novel reconfigurable architectures (FPGA, CGRA, etc.)
- Neural network acceleration on reconfigurable accelerators
- High-level synthesis on reconfigurable architectures
- Compilers for reconfigurable architectures
- Reconfigurable fabric security
- HW/SW prototyping and emulation on FPGAs
- Post-synthesis optimization for FPGAS
- FPGA-based prototyping for analog, mixed-signal, RF systems

1.6 Algorithms and Tools for Hardware Security

- New physical attack vectors or methods for ASICs
- Split Manufacturing for security
- Supply chain security and anti-counterieiting
- Artificial Intelligence for attack prevention systems
- Privacy-preserving computation

1.7 Architecture and Systems for Hardware Security

- Hardware Trojans, side-channel attacks, fault attacks and countermeasures
- Nano electronic security
- Hardware-based security (CAD for PUF's, RNG, AES etc.)
- Design and CAD for security
- Trusted execution environments
- Cloud Computing data security
- Sensor network security

1.8 Low Power and Approximate Computing

- Power and thermal estimation, analysis, optimization, and management techniques for hardware and software systems
- Energy- and thermal-aware application mapping and scheduling
- Energy- and thermal-aware architectures, algorithms
- Energy- and thermal-aware dark silicon system design
- Hardware techniques for approximate/stochastic computing

2) SYNTHESIS, VERIFICATION, PHYSICAL DESIGN, ANALYSIS, SIMULATION, AND MODELING

2.1 High-Level, Behavioral, and Logic

- High-level/Behavioral/Logic synthesis
- Technology-independent optimization and technology mapping
- Functional and logic timing ECO (engineering change order
- Resource scheduling, allocation, and synthesis
- Interaction between logic synthesis and physical design

2.2 Testing, Validation, Simulation, and Verification

- High-level/Behavioral/Logic modeling, validation, simulation
- Formal, semi-formal, and assertion-based verification
- Equivalence and property checking
- Emulation and hardware simulation/acceleration
- Post-silicon validation and debug
- Digital fault modeling and simulation Analysis and Optimization
- Delay, current-based, low-power test
- ATPG, BIST, DFT, and compression
- Memory test and repair
- Core, board, system, and 3D IC test

2.3 Cell-Library Design, Partitioning, Floorplanning, Placement

- Cell library design and optimization
- Transistor and gate sizing
- High-level physical design and synthesis
- Estimation and hierarchy management
- 2D and 3D partitioning. floorplanning, and placement
- Post-placement optimization
- Buffer insertion and interconnect planning

2.4 Clock Network Synthesis, Routing, and Post-Layout Optimization and Verification

- 2D and 3D clock network synthesis
- 2D and 3D global and detailed routing
- Package-/Board-level
- Chip-package-board co-design
- Post-layout/-silicon optimization
- Layout and routing issues for optical interconnects

2.5 Design for Manufacturability and Design for Synthesis and Optimization Reliability

- Process technology characterization, extraction, and modeling
- CAD for design/manufacturing interfaces
- CAD for reticle enhancement and lithography-related design
- Variability analysis and statistical design and optimization
- Yield estimation and design for yield
- Physical verification and design rule checking Verification
- Machine learning for smart manufacturing and process control
- Analysis and optimization for device-level reliability issues
- Analysis optimization for interconnect reliability issues
- Reliability issues related to soft errors
- Design for resilience and robustness

2.6 Timing, Power and Signal Integrity

- Deterministic and statistical static timing analysis, optimization
- Power and leakage analysis and optimization
- Circuit and interconnect-level low power design issues
- Power/ground network analysis and synthesis
- Signal integrity analysis and optimization

2.7 CAD for Analog/Mixed-Signal/RF and Multi-Domain Modeling

- Analog, mixed-signal, and RF noise modeling, simulation, test
- Electromagnetic simulation and optimization
- Device, interconnect and circuit extraction and simulation
- Behavior modeling of devices and interconnect
- Package modeling and analysis

3) CAD FOR EMERGING TECHNOLOGIES, PARADIGMS

3.1 Bio-inspired and Neuromorphic Computing

- Hardware for neuromorphic computing
- Event or spike-based hardware systems
- CAD for microfluidics
- CAD for biological computing systems
- CAD for synthetic biology
- CAD for bio-electronic devices, bio-sensors, MEMS

3.2 Nanoscale and Post-CMOS Systems

- New device structures and process technologies
- New memory technologies (flash, PCM, STT-RAM, memristor)
- Nanotechnologies, nanowires, nanotubes, graphene, étc.
- CAD for mixed-domain (semiconductor, nanoelectronic, MEMS, and electro-optical) devices, circuits, and systems
- CAD for nanophotonics and optical devices/communication
- CAD for field-coupled nanotechnologies
- Device, interconnect and circuit extraction and simulation
- Behavior modeling of devices and interconnect

3.3 New Computing Paradigm

- Non-von Neumann architectures
- Quantum computing

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SUBMISSION DETAILS

Paper submissions must be made through the online submission system at the **ICCAD website**.

Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage. Research papers with open-source software are highly encouraged where the software will be made publicly available (via GitHub or similar) with the camera-ready version if the paper has been accepted. For protecting the authors' identities in the double-blind review process, please do not include direct link to the non-anonymized software yet in the submitted paper but indicate the open-source contribution on a textural basis only. Authors wanting to share GitHub repositories may want to look into using **anonymous.4open.science** which is an open-source tool that helps you to quickly Double-blind your repository.

Authors are asked to submit their work in two stages. In stage one (abstract submission), a title, abstract, and a list of all co-authors must be submitted via the ICCAD web submission site. In stage two (paper submission), the paper itself is submitted whereby the submitted abstract of stage one can still be modified. Authors are responsible for **declaring COIs**, ensuring that their paper submission meets all guidelines, and that the PDF is readable.

DEADLINE FOR ABSTRACT AND PAPER SUBMISSIONS

The abstract submission deadline is Monday, May 15, 2023 at 23:59 AOE. No abstract submissions will be possible after this deadline.

The paper submission deadline is Monday, May 22, 2023 at 23:59 AOE.

We always have several authors contact the ICCAD office asking for a deadline extension. Due to the limited review cycle, NO extensions will be granted for ANY reason.

REGULAR PAPER SUBMISSIONS

- All papers must be in PDF format only, with savable text and embedded fonts in included (vector) graphics.
- Each paper must be no more than 8 pages (including the abstract, figures and tables), double-columned, 9pt or 10pt font. One page of references is allowed, which does not count towards this 8-page limitation.
- Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the author(s) own published works or affiliations should be made in the third person.
- Submissions not adhering to these rules, or determined to be previously published or simultaneously submitted to another conference, or journal, will be summarily rejected. Internal memoranda with full content not publicly available, and with author names not divulged, may be submitted.

IMPORTANT: Final camera-ready versions must be identical to the submitted papers with the following exceptions; inclusion of author names/affiliation, correction of identified errors, addressing reviewer demanded changes. No other modifications of any kind are allowed including modification of title, change of the author list, reformatting, restyling, rephrasing, removing figures/results/text, etc. The TPC Chairs reserve the right to finally reject any manuscripts not adhering to these rules.

TEMPLATES

Paper templates are available at the ICCAD website and authors are recommended to format their papers based on the IEEE template.

NOTIFICATION OF ACCEPTANCE

Authors will be notified of acceptance on or before, July 21, 2023. Final paper guidelines will be sent at that time.

PROCEEDINGS

The deadline for final camera-ready papers is August 14, 2023. Accepted regular papers are allowed six pages plus one page of references in the conference proceedings free of charge. Each additional page (except references) beyond six pages is subject to the page charge at $150.00 per page up to the eight-page plus one page of references. IEEE will hold the copyright for ICCAD 2023 proceedings. Authors of accepted papers must sign an IEEE copyright release form for their paper.

CONFERENCE REGISTRATION

At least one author per accepted regular paper or poster must be registered by August 18, 2023 in the conference. Failure to register will result in your paper being removed from the conference proceedings. In case of a regular paper, IEEE reserves the right to exclude a paper from distribution after the conference (e.g, removal from IEEE Digital Library) if the paper is not presented at the conference.

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ACM/IEEE WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

The awards are split into three categories. Two papers from this year's ICCAD conference, one from front-end and one from back-end, will receive

ACM/IEEE WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

Two papers from this year's ICCAD conference (one from front-end and one from back-end) will receive this prestigious award. The winners will be chosen from nominated papers after a thorough and competitive process by the area-specific selection committees and announced at the conference opening session

ICCAD TEN-YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

One paper from the 2013 and 2014 editions of ICCAD will be selected for the 10-year retrospective most influential paper award as evidenced by impact on the research community as reflected in citations, on the vendor community via its use in an industrial setting or on mew research venues as initiated by the paper during the past decade. Nominations from the community are welcome and can be sent to Robert Wile, Technical Program Vice Chair at robert.wille@tum.de.

CALL FOR PROPOSALS

Call for Workshop, Tutorial, Special Session, Panel and Keynote Proposals are all due on Monday May 22, 2023.

WORKSHOP PROPOSALS

ICCAD provides a vibrant and supportive environment for small-to-medium-sized affiliated workshops. Typical workshops are one-day events on the Thursday of ICCAD. All workshop proposals should be sent to Ismail Bustany, the Workshop Chair, at ismail.bustany@amd.com.

TUTORIAL PROPOSALS

AILICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and agood audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of bwo session blocks of 1.5-2 hours each) may be considered. Tutorial proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. Proposals should focus on the state-of-the-art in a specific area of broad interest amongst ICCAD attendees. All tutorial proposals should be submitted through the ICCAD website and questions can be addressed to Deming Chen, Tutorial and Special Sessions Chair, at dchen@illinois.edu. Please read the proposal guidelines at ICCAD website.

SPECIAL SESSION PROPOSALS

Special Sessions typically run 1.5-2 hours. Special session proposals should focus on in-depth treatment on a topic of timely interest to the ICCAD audience. Special session proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. All special session proposals should be submitted through the ICCAD website and questions can be addressed to Deming Chen, Tutorial and Special Sessions Chair, at dchen@illinois.edu. Please read the proposal guidelines at ICCAD website.

IF YOU NEED ASSISTANCE, PLEASE CONTACT THE APPROPRIATE COMMITTEE MEMBERS

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