



## TAU Workshop:

Each year ACM holds an international workshop on Timing Issues in the Specification and Synthesis of Digital Systems (Tau). The TAU workshop has been at the intersection of cutting-edge research and industry needs, drawing attendees from universities, foundries, design, CAD & Methodology teams of semiconductor and EDA companies around the world. The TAU workshops provide an informal forum for professionals working on the timing and performance domain of analog and digital systems to disseminate their work and to engage in a free discussion of ideas.

## Call for papers:

It has become clear that timing analysis and modeling is NO longer a solved problem. So, what are new challenges as the industry embraces 7/5/3nm and below, rides the wave of ultra-low-power mobile, computing accelerators for clouds service provider, wearable devices and jumps on the IoT bandwagon? Are there new issues with older nodes, 14/28nm and up, in new design use cases? How do we model timing/power interactions? How do reliability requirements coming from ADAS/IoT and related impact timing? How to we apply AI/ML/Data Science techniques to the timing domain? How do we meet the insatiable demands for accuracy, performance and functionality? What new fundamental challenges are coming from process physics, 3D, variability, voltage sensitivity, analog effects, Quantum circuit modeling, Ising Models, Mixed signal modeling and validation?

The twenty-eighth in the TAU series, the **TAU 2021** workshop invites submissions and proposals from the traditional as well as emerging areas related to the timing properties of digital electronic systems, including but not limited to the topics listed below.

- **Timing Simulation**
  - System/Gate/Transistor Level Timing Modeling & Analysis
  - Timing Corner optimization
  - Delay models and metrics
  - Reliability & Device aging Modeling
  - Silicon Correlation
  - Hierarchical Timing analysis
  - Timing Guard band & Margin
  
- **Variation analysis**
  - Timing analysis under uncertainty
  - Ultra-low voltage induced variation effects
  - Yield Analysis and Optimization
  - Statistical static timing analysis and optimization
  - Sensitivity Analysis
  - Clock skew optimization
  - Interconnect Variation Modeling





- **Power, Area, Cost trade-offs and optimization**
  - Timing challenges in low-power design
  - Timing driven layout optimization
  - Timing driven Physical Synthesis and Implementation
  - Low Power clock tree & network
- **Signal Integrity and Characterization**
  - Crosstalk modeling and analysis
  - Noise and glitch analysis
  - Simulation challenges of SRAM, dual edge flop, latch and new devices
  - Clock Synchronization Scheme
- **Others**
  - Timing Issues for 3D ICs, TSVs and Quantum Computation.
  - Usage of ML techniques
  - Asynchronous Systems
  - FPGA Design and Analysis
  - Smart Sensor Placement

### Important dates:

|   |                  |
|---|------------------|
| Paper submission: <a href="#">(Submission Open)</a> | <b>Dec, 2020</b> |
| Acceptance notification:                            | <b>Jan, 2021</b> |
| Camera ready paper due (for accepted papers):       | <b>Jan, 2021</b> |

### Submission of papers:

All papers (including invited papers and camera-ready versions) must be submitted electronically using the EasyChair system at <https://easychair.org/conferences/?conf=tau2021>

In order to allow for a blind review, submitted pdf version of the papers should not contain the authors name or any direct reference to the authors. TAU is a workshop aimed at fostering a high level of professional interaction, not a conference. Copies of papers will be provided to the attendees, but the proceedings will not be published by the ACM or the IEEE. Therefore, accepted papers can still be submitted to other conferences and journals. For any question email to [tau.workshop.tpc@gmail.com](mailto:tau.workshop.tpc@gmail.com) or refer workshop's website <http://www.tauworkshop.com>

