EMBEDDED SYSTEMS WEEK EMBEDDED SYSTEMS WEEK



2018 ESWEEK PROGRAM SEPTEMBER 30 - OCTOBER 5

TORINO INCONTRA CONGRESS CENTER | ITALY

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WELCOME TO ESWEEK 2018



Soonhoi Ha | General Chair Seoul National Univ., Korea

Welcome to ESWEEK 2018 in Torino!

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of embedded systems and software. By bringing together three leading conferences (CASES, CODES+ISSS, EMSOFT), a special track on IoT (Internet of Things), two symposia (RSP, NOCS), and hot-topic workshops and tutorials. ESWEEK presents attendees a wide range of topics unveiling state of the art embedded systems design and HW/SW architectures. This year F1/10 challenge is also held as a special event.

Following the journal-integrated publication model started last year for the conferences CASES, CODES+ISSS, and EMSOFT, all regular papers presented in ESWEEK 2018 will be published in the IEEE Transactions on Computer –Aided Design of Integrated Circuits and Systems. To this end, the review process of the conferences was conducted in two stages with the opportunity of minor/major revisions before the final decision. Acceptance rates have been about 25.5% for all conferences with a total number of 270 submissions to the journal track. In addition, 50 Work-in-Progress track papers have been selected and will be published in the ESWEEK Proceedings.

The technical program on Monday, Tuesday, and Wednesday consists of 5 special sessions and 26 regular sessions from the three conferences. There is a strong emphasis on interaction as at the end of each session there is a poster presentation during which all presented papers can be discussed with the authors.

Like previous two years, we will make Tuesday a special IoT day, focusing on the newest developments in the "Internet of Things" (IoT) from an embedded systems point of view. A sequence of three sessions is exclusively devoted to this subject with contributions from all of the three conferences and one special session.

Highlights of the ESWEEK program are three distinguished keynote talks by prominent leaders in academia and industry, covering most relevant trends for future embedded systems and providing deep insights into technology drivers. Thomas A. Henzinger, president of IST(Institute of Science and Technology) Austria, presents a formal framework for specifying and monitoring rich temporal properties of real-valued signals and its application to micro-electronics: "The First-Order Logic of Signals." Ahmad-Reza Sadeghi from the TU Darmstadt, Germany will address various security and privacy challenges in the growing IoT landscape and a solution approach in the keynote: "Hitchhiker's Guide to the IoT Galaxy full of Security & Privacy Challenges (An Attempt)." Finally, the Wednesday keynote will be given by Dr. Jie Liu, Partner Research Manager and the GM of the Ambient Intelligent Team at Microsoft AI Perception and Mixed Reality, with the title "Outside-In Autonomous Systems".



Petru Eles | Vice-General Chair Linköping Univ., SE

The tutorials on Sunday precede the conferences and are an excellent opportunity to get in-depth knowledge in new trends and hot topics. There are four half-day tutorials and one full-day tutorial, covering a wide scope, from embedded machine learning and approximate computing up to manycore resource management, trustworthy microkernel, and schedulability analysis. As a special event, F1/10 Autonomous Racing Competition will be held on Monday after regular sessions complete, followed by three lunch tutorials from Monday to Wednesday on how to build, run, and race the F1/10 car. During the lunch hour on Monday and Tuesday, we will also have two industrial tutorials offered by industry sponsors. ARM and Xilinx. On Wednesday, we will initiate a special lunch meeting for women attendants, called "Women in ESWEEK", to encourage their contribution to embedded systems research.

Thursday and Friday are the days for the symposia and workshops. Besides two symposia, RSP (Rapid System Prototyping) and NOCS (Networks on Chip), we will have four workshops covering a wide range of important topics in embedded systems. They are Highly Efficient Neural Processing (HENP), INTelligent Embedded Systems Architecture and Applications (INTESA), Embedded Operating System Workshop (EWili), and a merger of Model-Based Design of Cyber Physical Systems (CyPhy) and Embedded and Cyber-Physical Systems Education(WESE). The conference program will conclude with the traditional panel on Wednesday afternoon focusing on "CPS: Here to stay or another fad?" Top experts from academia and industry will share their views on this controversial topic.

The organization of ESWEEK was only possible with the continuous support and help from many volunteers: The program chairs with their program committee members, the organizers of workshops, tutorials and symposia, all members of the organization committee, and last but not least, the local arrangements chairs and their team. Our special thank goes to the IEEE CEDA for their full support for our journal-integrated publication model of ESWEEK.

We are looking forward to meeting you at the inspiring and interesting ESWEEK 2018 in Torino!



GENERAL INFORMATION

Welcome to Torino

Torino (Turin in English) is an important business and cultural centre in northern Italy, capital of the Piedmont region, located mainly on the left bank of the Po River, surrounded by the western Alpine arch. The population of the urban area is estimated to be 1.7 million people. The city has a rich culture and history, and is known for its numerous art galleries, restaurants, churches, palaces, opera houses, city squares, parks, gardens, theatres, libraries, museums and other venues. Turin is well known for its baroque, rococo, neo-classical, and Art Nouveau architecture. Much of the city's public squares, castles, gardens and elegant palazzi such as Palazzo Madama, were built in the 16th and 18th century, after the capital of the Duchy of Savoy was moved to Turin from Chambéry (nowadays in France), as part of the urban expansion.

Torino is sometimes called the "cradle of Italian liberty", for having been the birthplace and home of notable politicians and people who contributed to the Renaissance, such as Cavour, a leading figure in the movement toward Italian unification, and many of the protagonists of Italian political and social life in the 20th century, among the others, Antonio Gramsci, Piero Gobetti, and Palmiro Togliatti. The city used to be a major European political centre, being Italy's first capital in 1861 and being home to the House of Savoy, the Italian royal family. The city currently hosts some of the best Italian universities, colleges, academies, such as the sixcenturier-old Univ. di Torino and the prestigeous Engineering school Politecnico di Torino. In addition to the Italian cuisine, the region around Torino offers some specialties that include: a variety of cheese from the neighboring mountains. Dessert traditions include creative uses of hazelnuts cream. The region has seen the birth of internationally recognized movements, such as SlowFood, and of the Eataly "gourmet" grocery and restaurant chain. Torino is the home of several microbreweries, winners of international prizes every year.

Turin hosts prestigious museums and monuments, including the Egyptian Museum (the oldest museum entirely dedicated to Ancient Egypt and the second largest after Cairo's) and the Mole Antonelliana (featured on the Italian 2 cent euro coins). Turin's several monuments and sights make it one of the world's top 250 tourist destinations. Turin is also well known as the home of the Shroud of Turin, the football teams Juventus F.C. and Turin F.C., the headquarters of automobile manufacturers FIAT, Lancia and Alfa Romeo, and as host of the 2006 Winter Olympics. Several International Space Station modules, such as Harmony, Tranquility, and Columbus, were also manufactured at the Thales Alenia Space factory in Turin.

Turin is the only Italian city enlisted in the New York Times "52 Places to Go in 2016" guide.

Conference Registration Fees

Conference registration allows attendance to any of the three ESWEEK conferences, CODES+ISSS, CASES, and EMSOFT. Conference registration includes lunch on conference days, online conference proceedings, the Sunday Welcome Reception, and one ticket to the banquet. Student Conference registration does not include a banquet ticket, but one can be purchased. Workshops, Tutorials, and Symposia can be added on to your registration for an additional fee.

Conference Member	\$900		
Conference Non-Member	\$1000		
Conference Student Member	\$450		
Conference Student Non-Member	\$600		
One Day Workshop Member	\$350		
One Day Workshop Student	\$250		
Two Day Workshop Member	\$400		
Two Day Workshop Student	\$300		
Symposia			
NOCS Member	\$550		
NOCS Student	\$380		
RSP Member	\$400		
RSP Student	\$300		





ESWEEK 2018 OVERVIEW

Sunday, September 30

Welcome Reception

Tutorials

Monday, October 1

Opening Session

Keynote by Thomas Henzinger

CASES, CODES+ISSS, & EMSOFT Sessions

Poster Sessions

Technical Program Committee Dinner

Tuesday, October 2

Keynote by Ahmad-Reza Sadeghi

CASES, CODES+ISSS, EMSOFT & IoT Day Sessions

Poster Sessions

Social Event - Museo Nazionale del Risorgimento Italiano

Wednesday, October 3

Keynote by Jie Liu

CASES, CODES+ISSS & EMSOFT Sessions

Poster Sessions

Best Paper Awards Ceremony

ESWEEK Panel

Thursday, October 4

EWiLi'18 Workshop HENP'18 Workshop INTESA'18 Workshop

CyPhy'18 Workshop

WESE'18 Workshop

NOCS'18 Symposium

RSP Symposium

Friday, October 5

EWiLi'18 Workshop HENP'18 Workshop NOCS'18 Symposium RSP Symposium



Conference Venue Floorplan









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BEST PAPER CANDIDATES

CASES

MINIMALLY BIASED MULTIPLIERS FOR APPROXIMATE INTEGER AND FLOATING-POINT MULTIPLICATION

Authors:

Hassaan Saadat - Univ. of New South Wales Haseeb Bokhari - Open Access Pty Ltd Sri Parameswaran - Univ. of New South Wales

HI-DMM: HIGH-PERFORMANCE DYNAMIC MEMORY MANAGEMENT IN HIGH-LEVEL SYNTHESIS

Authors:

Tingyuan Liang - Hong Kong Univ. of Science and Technology Jieru Zhao - Hong Kong Univ. of Science and Technology Liang Feng - Hong Kong Univ. of Science and Technology Sharad Sinha - Indian Institute of Technology Wei Zhang - Hong Kong Univ. of Science and Technology

DEEPTRAIN: A PROGRAMMABLE EMBEDDED PLATFORM FOR TRAINING DEEP NEURAL NETWORKS

Authors:

Duckhwan Kim - Georgia Institute of Technology Taesik Na - Georgia Institute of Technology Sudhakar Yalamanchili - Georgia Institute of Technology Saibal Mukhopadhyay - Georgia Institute of Technology

CODES + ISSS

XNOR NEURAL ENGINE: A HARDWARE ACCELERATOR IP FOR 21.6 FJ/ OP BINARY NEURAL NETWORK INFERENCE

Authors:

Francesco Conti - Eidgenössische Technische Hochschule Zürich & Univ. of Bologna Pasquale Davide Schiavone - Eidgenössische Technische Hochschule Zürich Luca Benini - Eidgenössische Technische Hochschule Zürich & Univ. of Bologna

MALOC: A FULLY PIPELINED FPGA ACCELERATOR FOR CONVOLUTIONAL NEURAL NETWORKS WITH ALL LAYERS MAPPED ON CHIP

Authors:

Lei Gong - Univ. of Science and Technology of China Chao Wang - Univ. of Science and Technology of China Xi Li - Univ. of Science and Technology of China Huaping Chen - Univ. of Science and Technology of China Xuehai Zhou - Univ. of Science and Technology of China

SYNTHESIS OF MONITORS FOR NETWORKED SYSTEMS WITH HETEROGENEOUS SAFETY REQUIREMENTS

Authors:

Mischa Möstl - Technische Univ. Braunschweig Johannes Schlatow - Technische Univ. Braunschweig Rolf Ernst - Technische Univ. Braunschweig

EMSOFT

TWO-LAYERED FALSIFICATION OF HYBRID SYSTEMS GUIDED BY MONTE CARLO TREE SEARCH

Authors:

Zhenya Zhang - National Institute of Informatics & Graduate Univ. for Advanced Studies Gidon Ernst - National Institute of Informatics Sean Sedwards - Univ. of Waterloo Ichiro Hasuo - National Institute of Informatics & Graduate Univ. for Advanced Studies

REAL-TIME DATA RETRIEVAL WITH MULTIPLE AVAILABILITY INTERVALS IN CPS UNDER FRESHNESS CONSTRAINTS Authors:

Chenchen Fu - City Univ. of Hong Kong Peng Wu - Univ. of Connecticut Minming Li - City Univ. of Hong Kong Jason Xue - City Univ. of Hong Kong Yingchao Zhao - Caritas Institute of Higher Education Song Han - Univ. of Connecticut

BOUNDING DRAM INTERFERENCE IN COTS HETEROGENEOUS MPSOCS FOR MIXED CRITICALITY SYSTEMS

Authors:

Mohamed Hassan - Univ. of Guelph & Intel Corporation Rodolfo Pellizzoni - Univ. of Waterloo



SUNDAY, SEPTEMBER 30 TUTORIALS SCHEDULE

	Giolitti	Einaudi	Sella	
09:00 - 13:00	Embedded Machine Learning Today and Tomorrow	Spectrum of Run- time Management for Modern and Next Generation Multi/ Many-core Systems	Schedulability Analysis Under Uncertainty Using Formal Methods	
13:00 - 14:00	Lunch Room: Torino Hall			
14:00 - 18:00	Kickstarting Developing on seL4, the World's Most Trustworthy and Difficult to Work With Microkernel	A Comprehensive Analysis of Approximate Computing Techniques: From Component- to Application-Level	Schedulability Analysis Under Uncertainty Using Formal Methods	
18:30	Welcome Reception Caffe' Torino			



SUNDAY, SEPTEMBER 30 - TUTORIALS

Tutorial 1 - Embedded Machine Learning Today and Tomorrow Time: 9:00 - 13:00 | Room: Giolitti

Organizer:

Luca Benini - ETH Zürich & Univ. of Bologna

The tutorial will start with an overview of architectures and systems for machine learning available today, with a focus on advanced techniques to boost energy efficiency for ML accelerators, such as

exploiting temporal redundancy, sparsity and reduced precision in inference and training. We will then cover some of the recent progress and challenges in implementing machine learning algorithms using

analog resistive memory devices. Finally, we will discuss spiking neural networks and the properties and advantages that are unique to them, including new algorithms applied on spatiotemporal data. The emulation of these bio-inspired mechanisms, through the physics of nanodevices, particularly memristors, will be covered.

BIOGRAPHIES:

Luca Benini holds the chair of digital Circuits and systems at ETHZ and is Full Professor at the Universita di Bologna. He received ad PhD degree from Stanford Univ. in 1997. Dr. Benini's research interests are in energy-efficient system design, from embedded to high-performance computing. He is also active in the design ultra-low power VLSI circuits for machine learning. He is a Fellow of the IEEE, of the ACM and a member of the Academia Europaea. He is the recipient of the 2016 IEEE CAS Mac Van Valkenburg award.

Lukas Cavigelli received the M.Sc. degree in electrical engineering and information technology from ETH Zürich, Zürich, Switzerland, in 2014. Since then he has been with the Integrated Systems Laboratory, ETH Zürich, where he is pursuing a PhD degree. His current research interests include deep learning, computer vision, embedded systems, and low-power integrated circuit design. He has received the best paper award at the VLSI-SoC and the ICDSC conferences in 2013 and 2017

and the best student paper award at the Security+Defense conference in 2016.

Manuel Le Gallo is a Post-Doctoral researcher at IBM Research - Zürich, where he is currently employed in the Memory and Cognitive Technologies group. His main research interest is in using phase-change memory devices for non-von Neumann computing. Manuel holds a doctoral degree in Electrical Engineering (DrSc) from ETH Zürich (2017), a Master's degree in Electrical Engineering and Information Technology (MSc) from ETH Zürich (2014), an undergraduate degree of Cycle Ingénieur Polytechnicien from Ecole Polytechnique Palaiseau, France (2014), as well as a Bachelor's degree in Engineering Physics (BEng) from Ecole Polytechnique de Montréal, Canada (2011).

Timoleon Moraitis is a researcher at IBM Research – Zürich, Switzerland, currently working on biologically-inspired machine learning algorithms such as spiking neural networks and their physical

implementation through hardware emulation. His research explores which neurosynaptic mechanisms can enable the next generation of cognitive machines. Previously he transitioned from the experimental and computational neuroscience of the rat's and human's sensory-motor system to neuromorphic engineering, during his PhD at the Institute of Neuroinformatics (INI) in Zürich. He received his diploma in applied mathematics and physics from the National Technical Univ. of Athens, Greece.

Speakers:

Luca Benini - *ETH Zürich & Univ. of Bologna* Lukas Cavigelli - *ETH Zürich* Timoleon Moraitis - *IBM Research* Manuel Le Gallo - *IBM Research*

Tutorial 2 - Spectrum of Run-time Management for Modern and Next Generation Multi/Many-core Systems *Time: 9:00 - 13:00 | Room: Einaudi*

Organizers:

Amit Kumar Singh - Univ. of Essex Geoff V. Merrett - Univ. of Southampton Akash Kumar - Technische Univ. Dresden Amir Rahmani - Univ. of California, Irvine

Run-time management of multi/many-core systems is becoming extremely challenging due to several factors, e.g. increasing demand to execute concurrent applications, inefficient exploitation of

heterogeneous cores, changing workload variations over time, changing run-time scenarios and desire for optimization of several metrics such as performance, energy consumption and reliability. For next

generation multi/many-core systems, the challenges will further increase mainly due to higher number of cores and increased heterogeneity.

This tutorial starts with a taxonomy of run-time management approaches, providing an overview of the field and comparing approaches. The attention then shifts to focus on a range of run-time power and energy management approaches. Thereafter, approaches considering reliability as their primarily optimization goal will be addressed. Finally, run-time management approaches that leverage multiple-input, multiple-output and supervisory control theory to offer scalable, autonomous, and coordinated resource management will be covered. Depending upon the target problems, the designers can employ these methodologies to achieve efficiency in multi/many-core systems in terms of performance, energy consumption and/or reliability.

BIOGRAPHIES:

Amit Kumar Singh is a Lecturer (Assistant Professor) at Univ. of Essex, UK. Previously, he worked as a post-doctoral researcher at Univ. of Southampton, UK from 2016 to 2017, at Univ. of York, UK from 2014 to 2016 and National Univ. of Singapore (NUS) from 2013 to 2014. He received the Ph.D. degree from Nanyang Technological Univ. (NTU), Singapore, in 2013. His current research interests include system level design-time and run-time optimizations of 2D and 3D multicore systems with focus on performance, energy, temperature, and reliability. Geoff V. Merrett is an Associate Professor at Univ. of Southampton, where he is head of the Centre for Internet of Things and Pervasive Systems. He received the PhD degree in Electronic Engineering from Southampton in 2009. He is internationally known for his research into the system-level energy management of mobile and self-powered embedded systems. He is currently a Co-Investigator on over £20M of UK-government-funded projects; for example 'PRiME' on energyefficient many-core computing systems. He is technical director of the Arm-ECS Research Centre, an award winning industry-academia collaboration between the Univ. of Southampton and ARM.

Akash Kumar is a Professor at Technische Universitat Dresden (TUD), Germany, where he is directing the chair for Processor Design. From 2009 to 2015, he was with the Department of Electrical and Computer Engineering, NUS. He received the joint Ph.D. degree in electrical engineering in embedded systems from Univ. of Technology (TUe), Eindhoven and National Univ. of Singapore (NUS), in 2009. His current research interests include design, analysis, and resource management of low-power and fault-tolerant embedded multiprocessor systems.

Amir M. Rahmani is currently Marie Curie Global Fellow at Univ. of California Irvine (USA) and TU Wien (Austria). He is also an adjunct professor (Docent) in embedded parallel and distributed computing at the Univ. of Turku, Finland. He received the Ph.D. degree from Department of IT, Univ. of Turku, Finland, in 2012. He also received his MBA jointly from Turku School of Economics and European Institute of Innovation & Technology (EIT) ICT Labs, in 2014. His research interests span Self-aware Computing, Energy-efficient Many-core Systems, Runtime Resource Management, Healthcare Internet of Things, and Fog/Edge Computing.

Speakers:

Amit Kumar Singh - Univ. of Essex Geoff V. Merrett - Univ. of Southampton Akash Kumar - Technische Univ. Dresden Amir Rahmani - Univ. of California, Irvine



SUNDAY, SEPTEMBER 30 - TUTORIALS

Tutorial 3 - Schedulability Analysis Under Uncertainty Using Formal Methods Time: 9:00 - 18:00 | Room: Sella

Organizers:

Étienne André - *Univ. Paris 13* Giuseppe Lipari - *Univ. Lille*

Modern real-time systems must cope with different sources of variability. Modern hardware processors introduce several sources of variability in the execution time of the software (cache, pipeline, bus contention, etc.); and the timing of external events may change due to changes in the environments, malfunctions, etc. This variability adds additional challenges for the design, development and validation of modern cyber-physical systems. It is then necessary to estimate the robustness of the system w.r.t. variations of the parameters. A key issue is to estimate for which values of the parameters the system continues to meet all its timing constraints.

In this tutorial, we present the background for analyzing real-time systems using formal methods, and notably the formalism of parametric timed automata to analyze real-time scheduling under uncertainty. Then we will give a survey of some real-time scheduling problems, and we will show how to model a typical real-time system using the IMITATOR tool. The participants will be guided toward building and verifying a model of a real-time system, exploring the capability of the analysis tool.

BIOGRAPHIES:

Étienne André is an associate professor with Université Paris 13, France. His research interests include model checking real-time systems, notably in the presence of timing uncertainty, or unknown constants. He contributed to the field of parametric timed automata, and is the lead developer of IMITATOR, a state-of-the-art parametric model checker, applied in several industrial contexts (including ST-microelectronics, Astrium State Space transportation, and Thales). Web page: https://lipn.univ-paris13.fr/~andre/

Giuseppe Lipari is Professor of Computer Science at Univ. of Lille. He is head of the Embedded Real-Time Adaptative system Design and Execution (Émeraude) team of the Centre de Recherche en Informatique, Signal et Automatique (CRIStAL) de Lille. His research interests are in real-time systems, real-time operating systems, scheduling algorithms, embedded systems. He is an IEEE Fellow. Web page: http://cristal.univ-lille.fr/~lipari/

Speakers:

Étienne André - *Univ. Paris 13* Giuseppe Lipari - *Univ. Lille*

Tutorial 4 - Kickstarting Developing on seL4, the World's Most Trustworthy and Difficult to Work With Microkernel *Time:* 14:00 - 18:00 | *Room: Giolitti*

Organizers:

Anna Lyons - Univ. of New South Wales & Commonwealth Scientific and Industrial Research Organisation

Gernot Heiser - Univ. of New South Wales & Commonwealth Scientific and Industrial Research Organisation

seL4 is a microkernel offering unprecedented trustworthiness in the form of formal verification of correctness, integrity, isolation and a known WCET. This tutorial will kick-start everything you need to know to start working on seL4 and is in four parts: an introduction to seL4, hands on working with the kernel API and scheduling model, hands on use of rump kernels for basic POSIX support, and a presentation on how to set up Linux VMs with guest to guest communication.

BIOGRAPHIES:

Anna just submitted her PhD at UNSW which completely altered the seL4 scheduling model, offering for the first time a principled model for managing time in L4 kernels. She's now working as a senior engineer at CSIRO's Data61 and assisting with UNSW's Advanced Operating Systems course, which is based on seL4. Anna is interested in microkernel based OSes, trustworthy systems, practical real-time scheduling and teaching systems.

Gernot is Scientia Professor and John Lions Chair at UNSW Sydney, a Chief Research Scientist at CSIRO's Data61 and a Fellow of the IEEE, the ACM and the Academy of Technology and Engineering (ATSE). UNSW Gernot's main research interests are in operating systems, especially microkernel-based systems, and their use in critical systems; cyber-security, especially operating-system security; system trustworthiness and robustness; real-time systems; virtualisation; energy/power management and architectural support for operating systems Kofi is an engineer at UNSW working with CSIRO's Data61 on seL4 and the surrounding ecosystem. Kofi cares about coordinating the currently disjoint world of drivers, and unifying the Free and Open Source world and strengthening open-source operating system's ability to work with hardware vendors to get the drivers they need.

Kent is also an engineer at CSIRO's Data61. His interests include Systems engineering and how using different operating system architectures can help construct trustworthy applications. He has previously worked on efficient reuse of existing operating system services in alternative operating environments. In the near future he is interested in finding out how better temporal and spatial isolation can be used to build useful mixed-criticality trustworthy systems.

Speakers:

- Gernot Heiser Univ. of New South Wales & Commonwealth Scientific and Industrial Research Organisation
- Kofi Doku Atuah Univ. of New South Wales & Commonwealth Scientific and Industrial Research Organisation
- Kent McLeod Commonwealth Scientific & Industrial Research Organisation



SUNDAY, SEPTEMBER 30 - TUTORIALS

Tutorial 5 - A Comprehensive Analysis of Approximate Computing Techniques: From Component- to Application-Level

Time: 14:00 - 18:00 | Room: Einaudi

Organizers:

- Alberto Bosio Lyon Institute of Nanotechnology
- Daniel Menard Institut d'Électronique et de Télécommunications de Rennes
- Olivier Sentieys French Institute for Research in Computer Science and Automation

A new design paradigm, Approximate Computing (AxC), has been established to investigate how computing systems can be more energy efficient, faster, and less complex. Intuitively, instead of performing exact computation and, consequently, requiring a high amount of resources, AxC aims to selectively violate the specifications, trading accuracy off for efficiency. It has been demonstrated in the literature the effectiveness of imprecise computation for both software and hardware components implementing inexact algorithms, showing an inherent resiliency to errors.

This tutorial introduces basic and advanced topics on AxC. We intend to follow a bottom-up approach: from component- up to application-level. More in detail, we will first present the main concept and techniques (e.g., functional approximation, voltage over-scaling). We then move to present some compile-time results in terms of energy-efficiency, area, performance versus accuracy of computations when using customized arithmetic (fixed-point, floating-point) and also try to derive some conclusions by comparing the different paradigms. The algorithmic-level approximation methods are then presented. Energy consumption can be reduced by approximating or skipping part of the computation. The concept of incremental refinement, early termination and fast decision will be detailed.

BIOGRAPHIES:

Alberto Bosio received the PhD in Computer Engineering from the Politecnico di Torino, Italy in 2006. From 2007 he is an Associate Professor at LIRMM - Univ. of Montpellier in France. His research interests include Approximate Computing, In-Memory Computing, Test and Diagnosis of Digital circuits and systems and Reliability. He co-authored 1 book, 3 patents 35 journals, and over 120 conference papers. He will be the chair of the ETTTC from January 2018. He is a member of the IEEE. Web: http://www.lirmm.fr/~bosio/home/ Daniel Menard received the Ph.D. and HDR degrees in Signal Processing and Telecommunications from the Univ. of Rennes, respectively in 2002 and 2011. From 2003 to 2012 he was Associate Professor at Univ. of Rennes in France. He is currently Full Professor at INSA Rennes. His research activities focus on the energy efficient implementation of signal and image processing applications in embedded systems. His research topics include approximate computing, fixed-point arithmetic, energy optimization in MPSoC, low power HEVC video encoding and decoding and embedded stereo-vision. He has published 25 papers in international journals and 63 papers in international conferences. He is member of the DISPS Technical Committee of the IEEE Signal Processing Society. Web: http://dmenard.perso.insa-rennes.fr

Olivier Sentieys is a Professor at the Univ. of Rennes and holds an Inria Research Chair on Energy-Efficient Computing Systems. He has more than 20 years of expertise in the fields of system-on-chip architectures, reconfigurable systems and their associated CAD tools, finite arithmetic effects, numerical accuracy analysis and low-power sensor networks. He authored or coauthored more than 150 journal publications or peer-reviewed conference papers and hold 6 patents. In particular, his research on methods for analytical analysis of errors in reducedprecision arithmetic and word-length optimization since 2000 with more than 50 publications, can be considered as a pioneering work in the field of approximate computing.

Web: http://people.rennes.inria.fr/Olivier.Sentieys/

Speakers:

- Alberto Bosio Lyon Institute of Nanotechnology Daniel Menard - Institut d'Électronique et de Télécommunications de Rennes
- Olivier Sentieys French Institute for Research in Computer Science and Automation





MONDAY, OCTOBER 1 SCHEDULE OF EVENTS

	Cavour	Giolitti	Einaudi	
08:15 - 09:00	ESWEEK Opening Session Room: Cavour			
09:00 - 10:00	Monday Keynote: Thomas Henzinger - Institute of Science and Technology Austria, The First-Order Logic of Signals Room: Cavour			
10:00 - 10:30	Coffee Break Room: Foyer 1 & 2			
10:30 - 12:00	CASES: High-Level Synthesis	CODES+ISSS: Embedded Learning 1	EMSOFT: Hardware Management	
12:00 - 12:30	Poster Session			
12:30 - 14:00	Lunch Room: Torino Hall			
13:00- 13:45	F1/10 Tutorial Room: Sella ARM Tutorial Room: Einaudi			
14:00 - 15:30	CASES: Reconfigruable Architectures for Neural Networks	CODES+ISSS: Power-efficient Designs	EMSOFT: Runtime Monitoring and Numerical Stability	
15:30 - 16:00		Poster Session		
16:00 - 17:30	SPECIAL SESSION CODES+ISSS: Future Automotive Systems Design: Research Challenges and Opportunities	CODES+ISSS: Resilient Embedded Systems	EMSOFT: Hybrid Systems	
17:30 - 18:00		Poster Session		
17:30 - 18:30	3rd International F1/10	Autonomous Racing Competi	tion Room: Torino Hall	



Opening Session Time: 8:15 - 9:00 | Room: Cavour



Keynote: The First-Order Logic of Signals Time: 9:00 - 10:00 | Room: Cavour

Keynote Speaker: Thomas Henzinger - Institute of Science and Technology Austria

Formalizing properties of systems with continuous dynamics is a challenging task. In this paper, we propose a formal framework for specifying and monitoring rich temporal properties of real-valued signals. We introduce signal first-order logic (SFO) as a specification language that combines first-order logic with linear-real arithmetic and unary function symbols interpreted as piecewise-linear signals. We first show that while the satisfiability problem for SFO is undecidable, its membership and monitoring problems are decidable. We develop an offline monitoring procedure for SFO that has polynomial complexity in the size of the input trace and the specification, for a fixed number of quantifiers and function symbols. We show that the algorithm has computation time linear in the size of the input trace for the important fragment of bounded-response specifications interpreted over input traces with finite variability. We can use our results to extend signal temporal logic with first-order quantifiers over space and time parameters, while preserving its efficient monitoring. We finally demonstrate the practical appeal of our logic through a case study in the micro-electronics domain.

BIOGRAPHY:

Thomas A. Henzinger is president of IST Austria (Institute of Science and Technology Austria). He holds a Dipl.-Ing. degree in Computer Science from Kepler Univ. in Linz, Austria, an M.S. degree in Computer and Information Sciences from the Univ. of Delaware, a Ph.D. degree in Computer Science from Stanford Univ. (1991), and a Dr.h.c. from Fourier Univ. in Grenoble, France (2012) and from Masaryk Univ. in Brno, Czech Republic (2015). He was Assistant Professor of Computer Science at Cornell Univ. (1992-95), Assistant Professor (1996-97), Associate Professor (1997-98), and Professor (1998-2004) of Electrical Engineering and Computer Sciences at the Univ. of California, Berkeley. He was also Director at the Max-Planck Institute for Computer Science in Saarbruecken, Germany (1999) and Professor of Computer and Communication Sciences at EPFL in Lausanne, Switzerland (2004-09). His research focuses on modern systems theory, especially models, algorithms, and tools for the design and verification of reliable software, hardware, and embedded systems. His HyTech tool was the first model checker for mixed discrete-continuous systems. He is an ISI highly cited researcher, a member of Academia Europaea, a member of the German Academy of Sciences (Leopoldina), a member of the Austrian Academy of Sciences, a Fellow of the AAAS, a Fellow of the ACM, and a Fellow of the IEEE. He has received the Milner Award of the Royal Society, the Wittgenstein Award of the Austrian Science Fund, and an ERC Advanced Investigator Grant.

101.1 PAPER TITLE - KEYNOTE: THE FIRST-ORDER LOGIC OF SIGNALS

Alexey Bakhirkin - Univ. Grenoble Alpes Thomas Ferrere, Thomas A. Henzinger - Institute of Science and Technology Austria Dejan Nickovic - Austrian Institute of Technology





Session 1A - CASES: High-Level Synthesis Time: 10:30 - 12:00 | Room: Cavour

Chair:

Laura Pozzi - Univ. della Svizzera italiana

*1A.1 MINIMALLY BIASED MULTIPLIERS FOR APPROXIMATE INTEGER AND

FLOATING-POINT MULTIPLICATION

Hassaan Saadat - Univ. of New South Wales Haseeb Bokhari - Open Access Pty Ltd, Australia Sri Parameswaran - Univ. of New South Wales

*1A.2 HI-DMM: HIGH-PERFORMANCE DYNAMIC MEMORY MANAGEMENT IN

HIGH-LEVEL SYNTHESIS

Tingyuan Liang, Jieru Zhao, Liang Feng - Hong Kong Univ. of Science and Technology

Sharad Sinha - Indian Institute of Technology

Wei Zhang - Hong Kong Univ. of Science and Technology

1A.3 SLACKHAMMER: LOGIC SYNTHESIS FOR GRACEFUL ERRORS UNDER FREQUENCY SCALING

Tanfer Alan, Joerg Henkel - Karlsruhe Institute of Technology

Session 1B - CODES+ISSS: Embedded Learning 1

Time: 10:30 - 12:00 | Room: Giolitti

Chair:

Chengmo Yang - Univ. of Delaware

Co-Chair:

Franco Fummi - Univ. of Verona

1B.1 A DESIGN SPACE EXPLORATION FRAMEWORK FOR CONVOLUTIONAL

NEURAL NETWORKS IMPLEMENTED ON EDGE DEVICES Foivos Tsimpourlas, Lazaros Papadopoulos, Anastasios Bartsokas, Dimitrios Soudris - National Technical Univ. of Athens

*1B.2 XNOR NEURAL ENGINE: A HARDWARE ACCELERATOR IP FOR 21.6 FJ/ OP BINARY NEURAL NETWORK INFERENCE

Francesco Conti, Pasquale Davide Schiavone, Luca Benini -Eidgenössische Technische Hochschule Zürich & Univ. of Bologna

*1B.3 MALOC: A FULLY PIPELINED FPGA ACCELERATOR FOR CONVOLUTIONAL NEURAL NETWORKS WITH ALL LAYERS MAPPED ON CHIP

Lei Gong, Chao Wang, Xi Li, Huaping Chen, Xuehai Zhou - Univ. of Science and Technology of China

Session 1C - EMSOFT: Hardware Management

Time: 10:30 - 12:00 | Room: Einaudi

Chair:

Frank Müller - North Carolina State Univ.

*1C.1 BOUNDING DRAM INTERFERENCE IN COTS HETEROGENEOUS MPSOCS

FOR MIXED CRITICALITY SYSTEMS

Mohamed Hassan - Univ. of Guelph & Intel Corporation Rodolfo Pellizzoni - Univ. of Waterloo

1C.2 LIGHTWEIGHT, INTEGRATED DATA DEDUPLICATION FOR WRITE

STRESS REDUCTION OF MOBILE FLASH STORAGE Miao-Chiang Yen, Shih-Yi Chang, Li-Pin

Chang - National Chiao Tung Univ.

1C.3 THERMAL-AWARE RESOURCE MANAGEMENT FOR EMBEDDED REAL-TIME SYSTEMS

Youngmoon Lee - Univ. of Michigan

Hoon Sung Chwa - Daegu Gyeongbuk Institute of Science and Technology Kang Shin - Univ. of Michigan Shige Wang - General Motors Research and Development



Poster Session

Time: 12:00 - 12:30

Univ.

Session 2A- CASES: Reconfigruable Architectures for Neural Networks

Time: 14:00 - 15:30 | Room: Cavour

Chair:

Oliver Bringmann - Univ. of Tübingen

2A.1 GNA: RECONFIGURABLE AND EFFICIENT ARCHITECTURE FOR GENERATIVE NETWORK ACCELERATION

Jiale Yan, Shouyi Yin, Fengbin Tu, Leibo Liu, Shaojun Wei - *Tsinghua Univ.* & Institute of Microelectronics

2A.2 AUTO-TUNING CNNS FOR COARSE-GRAINED RECONFIGURABLE ARRAY-BASED ACCELERATORS

Inpyo Bae, Barend Harris, Hyemi Min, Bernhard Egger - Seoul National

2A.3 HETEROGENEOUS FPGA-BASED COST-OPTIMAL DESIGN FOR TIMING-CONSTRAINED CNNS

Weiwen Jiang - Chongqing Univ. & Univ. of Pittsburgh Edwin H.-M. Sha, Qingfeng Zhuge - East China Normal Univ. Lei Yang, Xianzhang Chen - Chongqing Univ. & Univ. of California, Irvine Jingtong Hu - Univ. of Pittsburgh

Session 2B - CODES+ISSS: Power-efficient Designs Time: 14:00 - 15:30 | Room: Giolitti

Chair: Roman Lysecky - Univ. of Arizona

2B.1 ENERGY-QUALITY-TIME OPTIMIZED TASK MAPPING ON DVFS-ENABLED MULTICORES

> Lei Mo - French Institute for Research in Computer Science and Automation Angeliki Kritikakou, Olivier Sentieys - Univ. of Rennes 1 & INRIA/IRISA

2B.2 ENERGY MANAGEMENT OF APPLICATIONS WITH VARYING RESOURCE USAGE ON SMARTPHONES

Anway Mukherjee, Thidapat Chantem -*Virginia Tech* 2B.3 DIGITAL FOVEATION: AN ENERGY-AWARE MACHINE VISION FRAMEWORK

Ekdeep S. Lubana - Indian Institute of Technology Roorkee Robert P. Dick - Univ. of Michigan & Stryd Inc

Session 2C - EMSOFT: Runtime Monitoring and Numerical Stability Time: 14:00 - 15:30 | Room: Einaudi

Chair:

Timothy Bourke - French Institute for Research in Computer Science and Automation

2C.1 AN ALGEBRAIC FRAMEWORK FOR RUNTIME VERIFICATION

Stefan Jakšić - Austrian Institute of Technology & Technische Univ. Wien Ezio Bartocci, Radu Grosu - Technische Univ. Wien Dejan Ničković - Austrian Institute of Technology

2C.2 DISCRETE CHOICE IN THE PRESENCE OF NUMERICAL UNCERTAINTIES

Debasmita Lohar, Eva Darulova - *Max Planck Institute for Software Systems* Sylvie Putot - *LIX, École Polytechnique* Eric Goubault - *Ecole Polytechnique*

2C.3 WORK-IN-PROGRESS: LIGHTWEIGHT DEADLOCK DETECTION TECHNIQUE FOR EMBEDDED SYSTEMS VIA OS-LEVEL ANALYSIS

Youngho Choi - Sungkyunkwan Univ. & Samsung Electronics, Visual Display Division

Jaeook Kwon, Seokjae Jeong, Hansub Park - Samsung Electronics, Visual Display Division

Young Ik Eom - Sungkyunkwan Univ.

2C.4 WORK-IN-PROGRESS: INTROSPECTION OF THE LINUX-BASED EMBEDDED FIRMWARES

Pavel Dovgalyuk, Natalia Fursova, Ivan Vasiliev Vladimir Makarov -Novgorod State Univ.

2C.5 WORK-IN-PROGRESS: DESIGN OF SECURITY-CRITICAL DISTRIBUTED REAL-TIME APPLICATIONS WITH FAULT-TOLERANT CONSTRAINT

Wei Jiang, Haibo Hu, Jinyu Zhan - Univ. of Electronic Science and Technology of China Ke Jiang - Veoneer

2C.6 WORK-IN-PROGRESS: FAST SNAPSHOT MIGRATION USING STATIC CODE INSTRUMENTATION

Jae-Yun Kim, Hyeon-Jae Lee, Soo-Mook Moon - *Seoul National Univ.*



Poster Session

Time: 15:30 - 16:00

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Special Session 3A: CODES+ISSS: Future Automotive Systems Design: Research Challenges and Opportunities *Time*: 16:00 - 17:30 | *Room: Cavour*

Chair:

Selma Saidi - Hamburg Univ. of Technology

Co-Chair:

Sebastian Steinhorst - Technische Univ. München

Organizers:

Selma Saidi - Hamburg Univ. of Technology Sebastian Steinhorst - Technische Univ. München Dirk Ziegenbein - Robert Bosch GmbH

Automotive systems are currently undergoing a radical shift in the way they are designed, implemented and deployed. Such changes impose an increased complexity and a high number of requirements in order to be more automated, connected, dependable and cost-effective. This raises several challenges that the embedded systems community has to face, encountered at different stages of systems development from modeling and design to software/hardware deployment and validation. This special session will be dedicated to invited speakers from industry to discuss current industrial trends and open problems in the hardware and software design of automotive systems, dictating rigorous constraints in terms of safety, real-time capabilities and security.

3A.1 BREAKING AUTOMOTIVE TRADITIONS ... BUT NOT THE LEGACY CODE Dirk Ziegenbein - Robert Bosch GmbH

3A.2 THE JOURNEY TOWARDS RECONCILING PERFORMANCE AND PREDICTABILITY

Gurulingesh Raravi - NVIDIA Corp.

3A.3 NEW CYBERSECURITY CHALLENGES IN A DISRUPTIVE AUTOMOTIVE WORLD

Marko Wolf - ESCRYPT

3A.4 PAPER TITLE - SPECIAL SESSION: FUTURE AUTOMOTIVE SYSTEMS DESIGN: RESEARCH CHALLENGES AND OPPORTUNITIES

Selma Saidi - Hamburg Univ. of Technology Sebastian Steinhorst - Technische Univ. München Arne Hamann - Bosch Research GmbH Dirk Ziegenbein - Robert Bosch GmbH Marko Wolf - ESCRYPT

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Session 3B - CODES+ISSS: Resilient Embedded Systems Time: 16:00 - 17:30 | Room: Giolitti

Chair:

Andreas Gerstlauer - Univ. of Texas at Austin

*3B.1 SYNTHESIS OF MONITORS FOR NETWORKED SYSTEMS WITH HETEROGENEOUS SAFETY REQUIREMENTS

Mischa Möstl, Johannes Schlatow, Rolf Ernst - Technische Univ. Braunschweig

3B.2 TRADING-OFF ACCURACY AND ENERGY OF DEEP INFERENCE ON EMBEDDED SYSTEMS: A

CO-DESIGN APPROACH

Nitthilan Kannappan Jayakodi, Anwesha Chatterjee, Wonje Choi, Janardhan Rao Doppa, Partha Pratim Pande - *Washington State Univ.*

3B.3 WORK-IN-PROGRESS: COMMUNICATION OPTIMIZATION FOR

THERMAL RELIABLE OPTICAL NETWORK-ON-CHIP

Mengquan Li - Chongqing Univ. Weichen Liu - Nanyang Technological Univ. Lei Yang - Chongqing Univ. Yiyuan Xie - Southwest Univ. Yaoyao Ye - Shanghai Jiao Tong Univ. Nan Guan - Hong Kong Polytechnic Univ.

3B.4 WORK-IN-PROGRESS: INTRODUCING ASSUME-GUARANTEE CONTRACTS FOR VERIFYING ROBOTIC APPLICATIONS

Stefano Spellini - Univ. of Verona Michele Lora, Sudipta Chattopadhyay - Singapore University of Technology and Design & Univ. of Verona Franco Fummi - Univ. of Verona

3B.5 WORK-IN-PROGRESS: DYNAMIC DATA MANAGEMENT FOR AUTOMOTIVE ECUS WITH HYBRID RAM-NVM MEMORY

Jinyu Zhan, Junhuan Yang, Wei Jiang, Yixin Li - Univ. of Electronic Science and Technology of China

3B.6 WORK-IN-PROGRESS: SECURE NON-VOLATILE MEMORY WITH SCRATCH PAD MEMORY USING DUAL ENCRYPTION MODE

Thomas Haywood Dadzie - Hanyang Univ. Jihye Kim - Kookmin Univ. Hyunok Oh - Hanyang Univ.

3B.7 WORK-IN-PROGRESS: RUNTIME REQUIREMENTS MONITORING FOR

STATE-BASED HARDWARE

Minjun Seo, Roman Lysecky - Univ. of Arizona



Session 3C - EMSOFT: Hybrid Systems Time: 16:00 - 17:30 | Room: Einaudi

Chair:

Indranil Saha - Indian Institute of Technology Kanpur

*3C.1 TWO-LAYERED FALSIFICATION OF HYBRID SYSTEMS GUIDED BY MONTE CARLO TREE SEARCH

Zhenya Zhang, Gidon Ernst - National Institute of Informatics & Graduate Univ. for Advanced Studies Sean Sedwards - Univ. of Waterloo Ichiro Hasuo - National Institute of Informatics & Graduate Univ. for Advanced Studies

3C.2 SAFETY VERIFICATION OF NONLINEAR HYBRID SYSTEMS BASED ON

BILINEAR PROGRAMMING

Yifan Zhang - *Nanjing Univ.* Zhengfeng Yang - *East China Normal Univ.* Wang Lin - *Zhejiang Sci-Tech Univ.* Huibiao Zhu - *East China Normal Univ.* Xin Chen, Xuandong Li - *Nanjing Univ.*

3C.3 FORMAL FEATURE INTERPRETATION OF HYBRID SYSTEMS

Antonio A. Bruto da Costa - Indian Institute of Technology Kharagpur Goran Frehse - Univ. of Grenoble & VERIMAG Pallab Dasgupta - Indian Institute of Technology Kharagpur

Poster Session

Time: 17:30 - 18:00

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3rd International F1/10 Autonomous Racing Competition

Time: 17:30 - 18:30 | *Room: Torino Hall*

Chair:

Marko Bertogna - Univ. of Modena and Reggio Emilia

CO-Chairs:

Madhur Behl - Virginia Polytechnic Institute and State Univ., Rahul Mangharam -Univ. of Pennsylvania

Organizers:

Mathew O. Kelly - Univ. of Pennsylvania, Varundev Sukhil - Virginia Polytechnic Institute and State Univ. Paolo Burgio - Univ. of Modena and Reggio Emilia

Houssam Abbas - Univ. of Pennsylvania

Madhur Behl - Virginia Polytechnic Institute and State Univ.

Rahul Mangharam - Univ. of Pennsylvania

Marko Bertogna - Univ. of Modena and Reggio Emilia

F1/10 is an international competition which exposes you to the foundations of perception, planning and control in a fun, and challenging environment. Participating teams race vehicles with similar hardware specification and try to

outsmart, and outpace each other in a battle of algorithms. Many former F1/10 race engineers are now employed in Tesla's AutoPilot group, Nvidia's DrivePX AV group, Ford's AV group, among others.

At ESWeek we will have more cars, higher speeds, and some wheel-to-wheel autonomous racing action.



	Cavour	Giolitti	Einaudi	Sella
09:00 - 10:00	Tuesday Keynote: Ahmad-Reza Sadeghi -Hitchhiker's Guide to the IoT Galaxy full of Security & Privacy Challenges (An Attempt) Room: Cavour			
10:00 - 10:30	Coffee Break Room: Foyer 1 & 2			
10:30 - 12:00	CASES: Architectures and Compilers for Real-Time Systems	CODES+ISSS: Embedded Learning 2	EMSOFT: Automata	IoT TRACK: Edge Computing for IoT
12:00 - 12:30	Poster Session			
12:30- 14:00	Lunch Room: Torino Hall			
13:00- 13:45	F1/10 Tutorial Room: Sella Xilinx tutorial Room: Einaudi			
14:00- 1530	CASES: Neural Network Accelerators	CODES+ISSS: Flash Memories	EMSOFT: Real-Time Scheduling	IoT TRACK: Security and Efficiency of IoT Devices
15:30- 16:00	Poster Session			
16:00- 17:30	CASES: Efficient Memory and Storage	CODES+ISSS: Real-Time Systems	EMSOFT: Data Retrieval, Streaming, and Processing	SPECIAL SESSION IoT TRACK: The Future of IoT Security
17:30- 18:00	Poster Session			
19:00 - 21:00	Social Event at Museo Nazionale del Risorgimento Italiano			





Keynote: Hitchhiker's Guide to the IoT Galaxy Full of Security & Privacy Challenges (An Attempt) Time: 9:00 - 10:00 | Room: Cavour

Keynote Speaker: Ahmad-Reza Sadeghi - Technische Univ. Darmstadt

The Internet of things (IoT) is rapidly emerging with the goal to connect the unconnected. Many new device manufacturers are entering the market of internet-connected appliances for smart homes and offices, ranging from motion sensors to virtual voice assistants. However, due to lack of security by design and flawed implementations we are facing significant security and privacy challenges specific to IoT, such as perilous IoT botnet attacks, and novel privacy threats caused by widespread installation of wireless sensors, actuators and smart home appliances even in the private setting of our homes. Unfortunately, standard security measures like properly encrypted communications do not protect against these threats.

The massive scale of the IoT device population and enormous diversity of device hardware, operating systems, software frameworks and manufacturers makes it very difficult to establish standard IoT security and privacy-protecting solutions by simply applying and extending known solutions, neither for per-device security architectures nor for network security measures. In particular, existing intrusion detection techniques seem ineffective to detect compromised IoT devices.

In this talk, we will present our recent work, including industry collaborations, on addressing various security and privacy challenges in the growing IoT landscape. In particular, we focus on approaches for flexible management of devices security association (device pairing) as well as automated device identification and reliable detection of compromised devices based on their inherent communication behavior.

BIOGRAPHY:

Ahmad-Reza Sadeghi is a full professor of Computer Science at the TU Darmstadt, Germany. He is the head of the Systems Security Lab at the Cybersecurity Research Center of TU Darmstadt. Since 2012 he is also the director of the Intel Collaborative Research Institute for Secure Computing and Resilient Autonomous Systems at TU Darmstadt. He holds a Ph.D. in Computer Science from the Univ. of Saarland, Germany. Prior to academia, he worked in R&D of Telecommunications enterprises, amongst others Ericsson Telecommunications. He has been continuously contributing to security and privacy research. For his influential research on Trusted and Trustworthy Computing he received the renowned German "Karl Heinz Beckurts award. This award honors excellent scientific achievements with high impact on industrial innovations in Germany.

He has served as Editor-In-Chief of IEEE Security and Privacy Magazine, on editorial board of ACM Transactions on Information and System Security (TISSEC), and as guest editor of Transactions on Computer-Aided Design (TCAD), special Issue on Hardware Security and Trust. Currently he is serving on the editorial boards of ACM Security and Privacy Books, ACM Transactions on the Internet of Things (TIOT), and ACM Transactions on Design and Automation of Electronic Systems (TODAES).

108.1 PAPER TITLE - KEYNOTE: INTERNET OF THINGS OR THREATS? ON BUILDING TRUST IN IOT

Markus Miettinen, Ahmad-Reza Sadeghi - Technische Univ. Darmstadt





Session 4A - CASES: Architectures and Compilers for Real-Time Systems Time: 10:30 - 12:00 | Room: Cayour

Chair:

Andy Pimentel - Univ. of Amsterdam

4A.1 PREDICTABILITY AND PERFORMANCE AWARE REPLACEMENT POLICY PVISAM FOR UNIFIED SHARED CACHES IN REAL-TIME MULTICORES

Mohammad Shihabul Haque, Arvind Easwaran - Nanyang Technological Univ.

4A.2 A FAILURE RECOVERY PROTOCOL FOR SOFTWARE-DEFINED REAL-TIME NETWORKS

Tao Qian, Frank Mueller - *North Carolina* State Univ.

4A.3 ANALYZING DATA CACHE RELATED PREEMPTION DELAY WITH MULTIPLE PREEMPTIONS

Wei Zhang, Nan Guan - *Hong Kong Polytechnic Univ.* Lei Ju - *Shandong Univ.* Weichen Liu - *Nanyang Technological Univ.*

Session 4B - CODES+ISSS: Embedded Learning 2 Time: 10:30 - 12:00 | Room: Giolitti

Chair:

Mohammad Al Farugue - Univ. of California, Irvine

4B.1 POWER- AND ENDURANCE-AWARE NEURAL NETWORK TRAINING IN NVM-BASED PLATFORMS

Fanruo Meng, Yuan Xue, Chengmo Yang - Univ. of Delaware

4B.2 PRIORITY NEURON: A RESOURCE-AWARE NEURAL NETWORK FOR CYBER-PHYSICAL SYSTEMS

Maral Amir, Tony Givargis - Univ. of California Irvine

Session 4C - EMSOFT: Automata

Time: 10:30 - 12:00 | Room: Einaudi

Chair:

Georgios Fainekos - Arizona State Univ.

4C.1 MOORE-MACHINE FILTERING FOR TIMED AND UNTIMED PATTERN MATCHING

Masaki Waga, Ichiro Hasuo - National Institute of Informatics

4C.2 THE OPACITY OF REAL-TIME AUTOMATA

Lingtai Wang, Naijun Zhan - Institute of Software, Chinese Academy of Sciences

4C.3 WORK-IN-PROGRESS: DESIGN CONCEPT OF A LIGHTWEIGHT RUNTIME ENVIRONMENT FOR ROBOT SOFTWARE COMPONENTS ONTO EMBEDDED DEVICES

Hideki Takase, Tomoya Mori, Kazuyoshi Takagi, Naofumi Takagi - *Kyoto Univ.*

Session 4D - IoT: Edge Computing for IoT

Time: 10:30 - 12:00 | Room: Stella

Chair:

Chenyang Lu, Washington Univ.

4D.1 DEEPTHINGS: DISTRIBUTED ADAPTIVE DEEP LEARNING INFERENCE ON RESOURCE-CONSTRAINED IOT EDGE CLUSTERS

Zhuoran Zhao, Kamyar Mirzazad Barijough Andreas Gerstlauer - *Univ. of Texas at Austin*

4D.2 HOT-SPOT SUPPRESSION FOR RESOURCE-CONSTRAINED IMAGE RECOGNITION DEVICES WITH NON-VOLATILE MEMORY

Chun-Feng Wu - National Taiwan Univ. & Academia Sinica Ming-Chang Yang - The Chinese Univ. of Hong Kong Yuan-Hao Chang - Academia Sinica Tei-Wei Kuo - Academia Sinica & National Taiwan Univ.

4B.3 WEIGHTED QUANTIZATION-REGULARIZATION IN DNNS FOR WEIGHT MEMORY MINIMIZATION TOWARDS HW IMPLEMENTATION

Matthias Wess - Technische Univ. Wien & Siemens AG Sai Manoj Pudukotai Dinakarrao - George Mason Univ. Axel Jantsch - Technische Univ. Wien

4C.4 WORK-IN-PROGRESS: HIERARCHICAL CONTROL OF A CATOPTRIC SURFACE

Roger D. Chamberlain, Chandler Ahrens, Christopher Gill, Scott A. Mitchell - *Washington Univ.*

4C.5 WORK-IN-PROGRESS: ROAD CONTEXT-AWARE INTRUSION DETECTION SYSTEM FOR AUTONOMOUS CARS

Tanya Srivastava, Pryanshu Arora - *Birla Institute of Technology & Science* Chundong Wang, Sudipta Chattopadhyay - *Singapore Univ. of Technology and Design*

4C.6 WORK-IN-PROGRESS: TOWARDS OPTIMAL SCHEDULING OF THERMAL COMFORTABILITY AND SMOOTHENING OF LOAD PROFILE IN ENERGY EFFICIENT BUILDINGS

Nilotpal Chakraborty, Arijit Mondal, Samrat Mondal - Indian Institute of Technology Patna

4D.3 WORK-IN-PROGRESS: FOG COMPUTING FOR ADAPTIVE HUMAN-ROBOT COLLABORATION

Václav Struhár, Alessandro Vittorio Papadopoulos, Moris Behnam - Mälardalen Univ.

4D.4 WORK-IN-PROGRESS: HIERARCHICAL ENSEMBLE LEARNING FOR RESOURCE-AWARE FPGA COMPUTING

Hongfei Wang, Jianwen Li, Kun He, Wenjie Cai - *Huazhong Univ. of Science & Technology*



Poster Session

Time: 12:00 - 12:30

Session 5A - CASES: Neural Network Accelerators Time: 14:00-15:30 | Room: Cavour

Chair:

Bernhard Egger - Seoul National Univ.

*5A.1 DEEPTRAIN: A PROGRAMMABLE EMBEDDED PLATFORM FOR TRAINING DEEP NEURAL NETWORKS

Duckhwan Kim, Taesik Na, Sudhakar Yalamanchili, Saibal Mukhopadhyay - Georgia Institute of Technology

5A.2 APPROXIMATE COMPUTING FOR LONG SHORT TERM MEMORY (LSTM)

NEURAL NETWORKS

Sanchari Sen, Anand Raghunathan - Purdue Univ.

Session 5B - CODES+ISSS: Flash Memories Time: 14:00-15:30 | Room: Giolitti

Chair:

Hyunok Oh - Hanyang Univ.

5B.1 WARD: WEAR AWARE RAID DESIGN WITHIN SSDS

Shunzhuo Wang, Fei Wu, Jiaona Zhou - *Huazhong Univ. of Science & Technology* Zhonghai Lu - *KTH Royal Institute of Technology*

Changsheng Xie - Huazhong Univ. of Science and Technology

5B.2 NVM-BASED FPGA BLOCK RAM WITH ADAPTIVE SLC-MLC CONVERSION

Lei Ju, Xiaojin Sui, Shiqing Li, Mengying Zhao - Shandong Univ. Chun Jason Xue - City Univ. of Hong Kong Jingtong Hu - Univ. of Pittsburgh Zhiping Jia - Shandong Univ.

5A.3 GRADIENT DESCENT USING STOCHASTIC CIRCUITS FOR EFFICIENT TRAINING OF LEARNING MACHINES

Siting Liu, Honglan Jiang - Univ. of Alberta Leibo Liu - Tsinghua Univ. Jie Han - Univ. of Alberta

5B.3 SCRUBBING-AWARE SECURE DELETION FOR 3D NAND FLASH

Wei-Chen Wang - Macronix International Co., Ltd. & National Taiwan Univ. Chien-Chung Ho - National Chung Cheng Univ. Yuan-Hao Chang - Academia Sinica Tei-Wei Kuo - National Taiwan Univ. Ping-Hsien Lin - Macronix International Co., Ltd.

Session 5C - EMSOFT: Real-Time Scheduling Time: 14:00-15:30 | Room: Einaudi

Chair:

Burcu Kulahcioglu Ozkan - Max Planck Institute for Software Systems

5C.1 EDF-VD SCHEDULING OF FLEXIBLE MIXED-CRITCALITY SYSTEM WITH MULTIPLE-SHOT TRANSITIONS

Gang Chen - Northeastern Univ. Nan Guan - The Hong Kong Polytechnic Univ. Biao Hu - Beijing Univ. of Chemical Technology Wang Yi - Uppsala Univ.

5C.2 A CAPACITY AUGMENTATION BOUND FOR REAL-TIME CONSTRAINED-DEADLINE PARALLEL TASKS UNDER GEDF

Jinghao Sun - Northeastern Univ. Nan Guan - The Hong Kong Polytechnic University & Univ. of Hong Kong Xu Jiang - The Hong Kong Polytechnic Univ. Shuangshuang Chang -Northeastern Univ. Zhishan Guo - Missouri Univ. of Science and Technology Qingxu Deng - Northeastern Univ.

5C.3 TOWARDS OVERHEAD-FREE INTERFACE THEORY FOR COMPOSITIONAL HIERARCHICAL REAL-TIME SYSTEMS

Jin Hyun Kim - Univ. of Pennsylvania Kyong Hoon Kim - Gyeongsang National Univ. Arvind Easwaran - Nanyang Technological Univ. Insup Lee - Univ. of Pennsylvania

Wang Yi - Uppsala Univ.

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Session 5D - IoT: Security and Efficiency of IoT Devices Time: 14:00-15:30 | Room: Stella

Chair:

Andreas Gerstlauer - Univ. of Texas at Austin

5D.1 ASSURED: ARCHITECTURE FOR SECURE SOFTWARE UPDATE OF REALISTIC EMBEDDED DEVICES

N. Asokan, Thomas Nyman - Aalto Univ. & Trustonic Norrathep Rattanavipanon - Univ. of California, Irvine Ahmad-Reza Sadeghi - Technische Univ. Darmstadt Gene Tsudik - Univ. of California, Irvine

5D.2 ENZYME: AN ENERGY EFFICIENT TRANSIENT COMPUTING PARADIGM FOR ULTRA-LOW SELF-POWERED IOT EDGE DEVICES

Chen Pan, Mimi Xie, Jingtong Hu - Univ. of Pittsburgh

5D.3 WORK-IN-PROGRESS: ENHANCED RESILIENT SENSOR ATTACK DETECTION USING FUSION INTERVAL AND MEASUREMENT HISTORY

Kang Yang, Rui Wang - Capital Normal Univ. Yu Jiang - Tsinghua Univ. Chenxia Luo, Yong Guan, Xiaojuan Li, Zhiping Shi - Capital Normal Univ.

5D.4 WORK-IN-PROGRESS: A CHIP-LEVEL SECURITY FRAMEWORK FOR ASSESSING SENSOR DATA INTEGRITY

Taimour Wehbe, Vincent Mooney, David Keezer - Georgia Institute of Technology

WORK-IN-PROGRESS: VERTICALTHINGS - A LANGUAGE-BASED 5D.5 MICROKERNEL FOR CONSTRAINED IOT DEVICES Jayaraj Poroor - Amrita Vishwa Vidyapeetham

Poster Session

Time: 15:30-16:00

Session 6A - CASES: Efficient Memory and Storage Time: 16:00-17:30 | Room: Cavour

Chair:

Lars Bauer - Karlsruhe Institute of Technology

6A.1 EXTENDING FLASH LIFETIME IN EMBEDDED PROCESSORS BY EXPANDING ANALOG CHOICE

Georgios Mappouras - Duke Univ. Alireza Vahid - Univ. of Colorado, Denver Robert Calderbank, Daniel J. Sorin - Duke Univ.

6A.2 MCDRAM: LOW LATENCY AND ENERGY-EFFICIENT MATRIX COMPUTATIONS IN DRAM

Hyunsung Shin - Samsung Electronics Co., Ltd. Dongyoung Kim, Eunhyeok Park - Seoul National Univ. Sungho Park, Yongsik Park - Samsung Electronics Sungjoo Yoo - Seoul National Univ.

WORK-IN-PROGRESS: MAXIMIZING I/O THROUGHPUT AND MINIMIZING PERFORMANCE VARIATION VIA REINFORCEMENT LEARNING **BASED I/O MERGING FOR SSDS**

Wu Chao, Cheng Ji, Qiao Li, Chenchen Fu, Chun Jason Xue, Chenchen Fu - City Univ. of Hong Kong

6A.4 WORK-IN-PROGRESS: PERSISTENCE IMPROVEMENT FOR DISTRIBUTED CACHE WITH NVM BASED STORAGE SYSTEM

Junlong Wang, Wei Jiang, Jinyu Zhan - Univ. of Electronic Science and Technology of China Jinhuan Yu - City Univ. of Hong Kong Haibo Hu, Liugen Xu - Univ. of Electronic Science and Technology of China

WORK-IN-PROGRESS: MULTIPLE ALIGNMENT OF PACKET 6A.5 SEQUENCES FOR EFFICIENT COMMUNICATION IN A MANY-CORE NEUROMORPHIC SYSTEM

Gianvito Urgese, Luca Peres, Francesco Barchi, Enrico Macii, Andrea Acquaviva - Politecnico di Torino

6A.6 WORK-IN-PROGRESS: IMPACT OF GRAPH PARTITIONING ON SNN

PLACEMENT FOR A MULTI-CORE NEUROMORPHIC ARCHITECTURE Francesco Barchi, Gianvito Urgese, Enrico Macii, Andrea Acquaviva -Politecnico di

6A 7 ERROR-RESILIENCE IN CIRCUITS

Ilaria Scarabottolo, Giovanni Ansaloni, Laura Pozzi - Univ. della Svizzera italiana

Session 6B - CODES+ISSS: Real-Time Systems Time: 16:00-17:30 | Room: Giolitti

Chair:

Jason Xue - City Univ. of Hong Kong

6B.1 RESOURCE OPTIMIZATION FOR REAL-TIME STREAMING APPLICATIONS USING TASK REPLICATION

Sobhan Niknam, Peng Wang, Todor Stefanov - Leiden Univ.

6B.2 EOMESH: COMBINED FLOW BALANCING AND DETERMINISTIC ROUTING FOR REDUCED WCET ESTIMATES IN EMBEDDED REAL-TIME SYSTEMS

Jordi Cardona, Carles Hernandez, Jaume Abella, Francisco J. Cazorla -Barcelona Supercomputing Center

6B.3 WORK-IN-PROGRESS: HARDWARE IMPLEMENTATION OF A MULTI-MODE-AWARE MIXED-CRITICALITY SCHEDULER

Sena Hounsinou, Aishwarya Vasu - Southern Illinois Univ. Carbondale Harini Ramaprasad - Univ. of North Carolina

6B.4 WORK-IN-PROGRESS: CO-DESIGN OF SECURITY-CRITICAL REAL-TIME SYSTEMS TO PREVENT FAULT INJECTION ATTACKS

Wei Jiang, Liugen Xu, Jinyu Zhan - Univ. of Electronic Science and Technology of China Ke Jiang - Veoneer

6B.5 WORK-IN-PROGRESS: REVISITING WEAR LEVELING DESIGN ON COMPRESSION APPLIED 3D NAND FLASH MEMORY

Yejia Di, Liang Shi, Congming Gao-Chongging Univ. Qiao Li, Jason Xue - City Univ. of Hong Kong

6B.6 WORK-IN-PROGRESS: EQUIVALENCE OF TRANSFORMATIONS OF SYNCHRONOUS DATA FLOW GRAPHS

Xue-Yang Zhu - Institute of Software, Chinese Academy of Sciences

6B.7 WORK-IN-PROGRESS: QUANTIZED NNS AS THE DEFINITIVE SOLUTION FOR INFERENCE ON LOW-POWER ARM MCUS? Manuele Rusci, Alessandro Capotondi, Francesco Conti, Luca Benini -Univ. of Bologna & Swiss Federal Institute of Technology

Torino WORK-IN-PROGRESS: A PARTITIONING STRATEGY FOR EXPLORING



Session 6C - EMSOFT: Data Retrieval, Streaming, and Processing

Time: 16:00-17:30 | Room: Einaudi Chair:

Houssam Abbas - Oregon State Univ.

*6C.1 REAL-TIME DATA RETRIEVAL WITH MULTIPLE AVAILABILITY INTERVALS IN CPS UNDER FRESHNESS CONSTRAINTS

Chenchen Fu - City Univ. of Hong Kong Peng Wu - Univ. of Connecticut Minming Li, Jason Xue - City Univ. of Hong Kong Yingchao Zhao - Caritas Institute of Higher Education Song Han - Univ. of Connecticut

6C.2 OPTIMIZING GRAPH ALGORITHMS IN ASYMMETRIC MULTICORE PROCESSORS

Jyothi Krishna V S, Rupesh Nasre - Indian Institute of Technology Madras

MODELING, ANALYSIS, AND HARD REAL-TIME SCHEDULING OF 60.3 ADAPTIVE STREAMING APPLICATIONS

Jiali Teddy Zhai, Sobhan Niknam, Todor Stefanov- Leiden Univ.

Session 6D Special Session: IoT: The Future of IoT Security Time: 16:00-17:30 | Room: Stella

Chair:

Sibin Mohan - Univ. of Illinois at Urbana-Champaign

Organizer:

Sibin Mohan - Univ. of Illinois at Urbana-Champaign

The Internet-of-Things (IoT) is a large and complex domain. These systems are often constructed using a very diverse set of hardware, software and protocols. This, combined with the ever increasing number of IoT solutions/services that are rushed to market means that most such systems are rife with security holes. Recent incidents (eg the Mirai botnet) further highlight such security issues.

With emerging technologies such as blockchain and software-defined networks (SDNs), new security solutions are possible in the IoT domain. In this paper we will explore future trends in IoT security: (a) the use of blockchains in IoT security, (b) data provenance for sensor information, (c) reliable and secure transport mechanisms using SDNs (d) scalable authentication and remote attestation mechanisms for IoT devices and (e) threat modeling and risk/maturity assessment frameworks for the domain.

- BLOCKCHAINS FOR IOT SECURITY 6D.1 Mikael Asplund - Linköping Univ.
- TRUSTWORTHY SENSOR DATA 6D.2 Gedare Bloom - Howard Univ
- SCALABLE AUTHENTICATION FOR IOT DEVICES 6D.3 Negin Salajageh - Visa Research
- **REMOTE ATTESTATION FOR IOT DEVICES** 6D.4 Ahmad-Reza Sadeghi - Technische Univ. Darmstadt
- THREAT, RISK AND MATURITY ASSESSMENT FRAMEWORK FOR IOT 6D.5 Bruno Sinopoli - Carnegie Mellon Univ.
- PAPER TITLE SPECIAL SESSION: THE FUTURE OF IOT SECURITY 6D.6 Sibin Mohan - Univ. of Illinois at Urbana-Champaign Mikael Asplund - Linköping Univ. Gedare Bloom - Howard Univ. Ahmad-Reza Sadeghi, Ahmad Ibrahim - Technische Univ. Darmstadt Negin Salajageh - Visa Research Paul Griffioen, Bruno Sinopoli - Carnegie Mellon Univ.

Poster Session Time: 17:00 - 17:30

Social Event at Museo Nazionale del Risorgimento Italiano Time: 19:00 - 21:00



WEDNESDAY, OCTOBER 3 SPECIAL EVENTS

	Cavour		Einaudi	Sella
09:00 - 10:00	Wednesday Keynote: Jie Liu - Microsoft Research: Outside-In Autonomous Systems Room: Cavour			
10:00 - 10:30	Coffee Break Room: Foyer 1 & 2			
10:30 - 12:00	CASES: Embedded Systems Security	CODES+ISSS: Embedded System Design Tools	EMSOFT: Autonomous Systems	SPECIAL SESSION EMSOFT: Embedded Software for Robotics: Challenges and Future Directions
12:00 - 12:30	Poster Session			
12:30- 14:00	Lunch Room: Torino Hall			
12:30- 14:00	Women in ESWEEK meeting Room: Sala Stampa			
13:00- 13:45	F1/10 Tutorial Lunch Room: Sella			
14:00- 15:30	CASES: Cache Memory Management	Special Session CODES+ISSS: Design and Deployment of Advanced Driver Assistance Systems in Ground Vehicles	EMSOFT: Verification	
15:30- 16:00	Poster Session			
16:00- 17:30	Special Session CASES: Towards Secure Computer Architecture: Understanding Security Vulnerabilities and Emerging Attacks for Better Defenses	CODES+ISSS: Embedded Accelerators	EMSOFT: End-to-End Latency	
17:30- 18:00	Poster Session			
18:00- 18:15	Best Paper Awards Ceremony			
18:15- 19·45	Panel: Future of CPS: Here to stay or another fad? Room: Cavour			





Keynote: Outside-In Autonomous Systems *Time:* 9:00 - 10:00 | *Room: Cavour* Keynote Speaker:

Jie Liu - Microsoft Research

Breakthroughs in device intelligence promise autonomous systems that can achieve human level fidelity interacting with the physical world. While much attention has been focused on inside-out autonomous systems, such as selfdriving cars, AR goggles, and robots, which must cope with complex environments using primarily onboard sensing and computing capabilities, we argue the importance of its dual. Outside-in autonomous systems (OIAS) create smart environments that observe and understand space, people, and things from bird's eye points of view. In OIAS, people do not need to wear extra devices or to change their natural behaviors. Retail stores, factory floors, hospitals, and classrooms can all be augmented with various degrees of outside-in autonomy for better efficiency, higher productivity, and less mistakes.

We will discuss a few techniques, primarily on computer vision and sensor fusion, for building OIAS. These include people identification, people tracking, object identification, and activity recognition. We use autonomous retail stores as an example to illustrate current technology landscape and challenges of bringing lab-proven technologies to the real world. Due to their distributed, multi-modality and real-time nature, calibration, coordination and acceleration become keys for system scalability. Although fully autonomous systems still have a long way to go, technologies developed towards it can bring progressive values to live.

BIOGRAPHY:

Dr. Jie Liu is a Partner Research Manager and the GM of the Ambient Intelligent Team at Microsoft AI Perception and Mixed Reality. He is an IEEE Fellow, an ACM Distinguished Scientist and an ACM Distinguished Speaker. His research interests root in sensing and interacting with the physical world through computing. Examples include time, location, and energy awareness, and Internet/Intelligence of Things. He has published broadly in areas such as sensor networks, embedded systems, mobile and ubiquitous computing, and data center management, and has received 6 best paper awards in top academic conferences. In addition, he holds more than 100 patents. He is an Associate Editor of ACM Trans. on Sensor Networks; was an Associate Editor of IEEE Trans. on Mobile Computing; and has chaired a number of top-tier conferences and their steering committees, including CPS Week, IPSN, and SenSys. He obtained his Ph.D. degree from Electrical Engineering and Computer Sciences, UC Berkeley in 2001, and his Master and Bachelor's degrees from Department of Automation, Tsinghua Univ., Beijing, China. From 2001 to 2004, he was a research scientist in Palo Alto Research Center (formerly Xerox PARC)



Session 7A - CASES: Embedded Systems Security Time: 10:30 - 12:00 | Room: Cavour

Chair:

Ramesh Karri - New York Univ.

7A.1 FREQUENCY SCALING AS A SECURITY THREAT ON MULTICORE SYSTEMS

Philipp Miedl, Xiaoxi He, Matthias Meyer - *Eidgenössische Technische* Hochschule Zürich Davide Basilio Bartolini - Oracle Labs

Lothar Thiele - Eidgenössische Technische Hochschule Zürich

7A.2 GARUDA: DESIGNING ENERGY-EFFICIENT HARDWARE MONITORS FROM HIGH-LEVEL POLICIES FOR SECURE INFORMATION FLOW

Seaghan Sefton, Taiman Siddiqui, Nathaniel St. Amour, Gordon Stewart, Avinash Kodi - Ohio Univ.

7A.3 WORK IN PROGRESS: AN CONFIDENTIALITY AND INTEGRITY SCHEME FOR THE DISTRIBUTED SHARED MEMORY OF EMBEDDED MULTI-CORE SYSTEM

Pengfei Yang, Quan Wang, Xiaokun Huang, Xin Mi - Xidian Univ.

7A.4 WORK-IN-PROGRESS: GEMS: A GENERATOR FOR MODULO SCHEDULING PROBLEMS

Julian Oppermann, Sebastian Vollbrecht - Technische Univ. Darmstadt Melanie Reuter-Oppermann - Karlsruhe Institute of Technology Oliver Sinnen - Univ. of Auckland Andreas Koch - Technische Univ. Darmstadt

7A.5 WORK IN PROGRESS: COMMUNICATION-AWARE SCHEDULING OF DATA-PARALLEL TASKS

Kana Shimada - *Ritsumeikan Univ.* Ittetsu Taniguchi - *Osaka Univ.* Hiroyuki Tomiyama - *Ritsumeikan Univ.*

7A.6 WORK IN PROGRESS: PERFORMANCE MODELING FOR DATA DISTRIBUTION IN HETEROGENEOUS COMPUTING SYSTEMS.

Vanishree K, Madhura Purnaprajna - Amrita Vishwa Vidyapeetham

7A.7 WORK IN PROGRESS: EPERF: ENERGY-EFFICIENT EXECUTION OF USER-INTERACTIVE EVENT-DRIVEN APPLICATIONS Gaurav Chadha - Oracle America Inc

Session 7B - CODES+ISSS: Embedded System Design Tools Time: 10:30 - 12:00 | Room: Giolitti

Chairs:

Andy Pimentel - Univ. of Amsterdam, Daniel Muller Gritschneder - Technische Univ. München

7B.1 FORMAL MODELING AND VERIFICATION OF CONTROLLERS FOR A FAMILY OF DRAM CACHES

Debiprasanna Sahoo, Swaraj Sha, Manoranjan Satpathy - Indian Institute of Technology Bhubaneswar Madhu Mutyam - Indian Institute of Technology Madras Ramesh S - General Motors Research and Development Partha Roop - Univ. of Auckland

7B.2 SYNTHESIZABLE HIGHER-ORDER FUNCTIONS FOR C++ Dustin Richmond, Ryan Kastner, Alric Althoff - Univ. of California San Diego

Session 7C - EMSOFT: Autonomous Systems Time: 10:30 - 12:00 | Room: Einaudi

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Chair: Bai Xue - Chinese Academy of Sciences

7C.1 USING CONTROL SYNTHESIS TO GENERATE CORNER CASES: A CASE STUDY ON AUTONOMOUS DRIVING

Glen Chou, Yunus Sahin, Liren Yang, Kwesi Rutledge - Univ. of Michigan Petter Nilsson - California Institute of Technology Necmive Ozav - Univ. of Michiaan

7C.2 END-TO-END ANALYSIS AND DESIGN OF A DRONE FLIGHT CONTROLLER

Zhuoqun Cheng, Richard West, Craig Einstein - Boston Univ.

7B.3 PARAMETRIC CRITICAL PATH ANALYSIS FOR EVENT NETWORKS WITH MINIMAL AND MAXIMAL TIME LAGS

Joost van Pinxten, Marc Geilen - Eindhoven Univ. of Technology Martijn Hendriks - Netherlands Organisation for Applied Scientific Research

Twan Basten - Eindhoven Univ. of Technology

7C.3 SEMO: SERVICE-ORIENTED AND MODEL-BASED SOFTWARE FRAMEWORK FOR COOPERATING ROBOTS

Hyesun Hong - Seoul National Univ. Hanwoong Jung - Samsung Electronics KangKyu Park, Soonhoi Ha - Seoul National Univ.



Session 7D Special Session - EMSOFT: Embedded Software for Robotics: Challenges and Future Directions *Time: 10:30 - 12:00 | Room: Sella*

Organizers:

Houssam Abbas - Oregon State Univ. & Univ. of Pennsylvania Indranil Saha - Indian Institute of Technology Kanpur, Yasser Shoukry - Univ. of Maryland, College Park

Robots on the factory floor, on the streets, and in our homes, are being given increasing levels of autonomy. They inhabit the same physical environment as their human operators and users,

and must perform high-level cognitive tasks. These autonomous robots could enable autonomous transportation, autonomous medical devices and autonomous personal assistants. However, the complexity of their embedded software raises several challenges of guaranteeing safety, efficiency, and resiliency in accomplishing their high-level tasks. This special session highlights the challenges of the design and verification of embedded software for robotics. The presenters will address issues of control synthesis, adversarial testing, formal verification and efficient implementations of neural network code, and HW/SW real-time platforms for autonomous driving.

7D.1 THE ANTLAB SYSTEM FOR PROGRAMMING MULTI-ROBOT SYSTEMS Rupak Majumdar - *MPI-INF*

7D.2 SIMULATION-BASED ADVERSARIAL TEST GENERATION FOR EMBEDDED SOFTWARE IN AUTONOMOUS VEHICLES

Georgios Fainekos - Arizona State Univ.

Poster Session Time: 12:00 - 12:30

7D.3 ENERGY-EFFICIENT IMPLEMENTATIONS AND HARDWARE ACCELERATIONS OF NEURAL NETWORKS

Rajesh Gupta - Univ. of California

7D.4 SMT AND MILP VERIFICATION OF FEED FORWARD NEURAL NETWORKS

Rüdiger Ehlers - Univ. of Bremen

7D.5 HIGH-PERFORMANCE REAL-TIME PLATFORMS FOR AUTONOMOUS DRIVING SYSTEMS

Marko Bertogna - Univ. of Modena and Reggio Emilia

7D.6 PAPER TITLE - SPECIAL SESSION: EMBEDDED SOFTWARE FOR ROBOTICS: CHALLENGES AND FUTURE DIRECTIONS

Houssam Abbas - Univ. of Pennsylvania Indranil Saha - Indian Institute of Technology Kanpur Yasser Shoukry - Univ. of Maryland Rüdiger Ehlers - Univ. of Bremen Georgios Fainekos - Arizona State Univ. Rajesh Gupta - Univ. of California, San Diego Rupak Majumdar - MPI-INF Dogan Ulus - Boston Univ.





Session 8A - CASES: Cache Memory Management Time: 14:00-15:30 | Room: Cavour

Chair:

Amit Kumar Singh - Univ. of Essex

8A.1 CO-SCHEDULING ON FUSED CPU-GPU ARCHITECTURES WITH SHARED LAST LEVEL CACHES

Marvin Damschen - Karlsruhe Institute of Technology Frank Mueller - North Carolina State Univ. Joerg Henkel - Karlsruhe Institute of Technology

8A.2 SCRATCH THAT (BUT CACHE THIS): A HYBRID REGISTER CACHE / SCRATCHPAD FOR GPUS

Jonathan Bailey, John Kloosterman, Scott Mahlke - Univ. of Michigan

8A.3 WORK-IN-PROGRESS: WRITING-AWARE DATA VARIABLE ALLOCATION ON HYBRID SRAM+NVM SPM

Yixin Li, Jinyu Zhan, Wei Jiang, Ying Li - Univ. of Electronic Science and Technology of China

8A.4 WORK-IN-PROGRESS: DRAM CACHE ACCESS OPTIMIZATION LEVERAGING LINE LOCKING IN TAG CACHE

Shivani Tripathy, Debiprasanna Sahoo - Indian Institute of Technology Bhubaneswar Manoranjan Satpathy - Indian Institute of Technology, Bhubaneswar

8A.5 WORK-IN-PROGRESS: TOWARDS AUTOMATIC SCALAR REPLACEMENT IN OPENACC AND OPENMP PROGRAMS FOR GPU

Rokiatou Diarra, Alain Merigot, Bastien Vincke - Univ. of Paris Sud

8A.6 WORK-IN-PROGRESS: EXPLOITING SIMD CAPABILITY IN AN ARMV7-

TO-ARMV8 DYNAMIC BINARY TRANSLATOR

Sheng-Yu Fu, Chih-Min Lin - National Taiwan Univ. Ding-Yong Hong - Academia Sinica Yu-Ping Liu - National Taiwan Univ. Jan-Jan Wu - Academia Sinica Wei-Chung Hsu - National Taiwan Univ.

Session 8B Special Session - CODES+ISSS: Design and Deployment of Advanced Driver Assistance Systems in Ground Vehicles Time: 14:00-15:30 | Room: Giolitti

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Organizers:

Houssam Abbas - Univ. of Pennsylvania,

An Advanced Driver Assistance System (ADAS) automates various driving functions: from simple cruise control, to fully autonomous driving, via lanekeep assist, automatic emer- gency braking, highway driving and parking. ADAS present several grand challenges, that span the abstraction layers from hardware all the way up to applications and their incorporation into regulatory standards. The successful development of ADAS and autonomous vehicles requires a conversation between the engineers working at these different layers of abstraction.

- **8B.1** FORMAL VERIFICATION IN ADAS SYSTEMS Ramesh S - General Motors Company
- **8B.2 TESTING CLOSED-LOOP SYSTEMS WITH A NEURAL NETWORK** Tommaso Dreossi - Univ. of California, Berkeley
- 8B.3 THE DEVELOPMENT OF SAFETY BENCHMARKS FOR ADAS AND AUTONOMOUS VEHICLES Rahul Mangharam - Univ. of Pennsylvania
- **8B.4** AUTONOMOUS TRANSPORTATION SYSTEMS Adriano Alessandrini - Univ. of Florence

Session 8C- EMSOFT: Verification

Time: 14:00-15:30 | Room: Einaudi

Chair:

Tommaso Dreossi - Univ. of California, Berkeley

- 8C.1 AUTOMATIC VERIFICATION OF EMBEDDED SYSTEM CODE MANIPULATING DYNAMIC STRUCTURES STORED IN CONTIGUOUS REGIONS Jiangchao Liu, Liqian Chen - National Univ. of Defense Technology Xavier Rival - École Normale Supérieure & French Institute for Research in Computer Science and Automation
- 8C.2 SYMBOLIC VERIFICATION OF CACHE SIDE-CHANNEL FREEDOM Sudipta Chattopadhyay - Singapore Univ. of Technology and Design Abhik Roychoudhury - National Univ. of Singapore

8C.3 WORK-IN-PROGRESS: RTMUSRT: A REAL-TIME TESTBED FOR EMPIRICALLY COMPARING REAL-TIME MULTICORE SCHEDULERS Bo Wan, Bo Zhang, Xi Li, Kaiqi Zhou, Caixu Zhao, Chao Wang, Xuehai Zhou - Univ. of Science and Technology of China

8C.4 WORK-IN-PROGRESS: NVIDIA GPU SCHEDULING DETAILS IN VIRTUALIZED ENVIRONMENTS

Nicola Capodieci, Roberto Cavicchioli, Marko Bertogna - Univ. of Modena and Reggio Emilia

8C.5 WORK-IN-PROGRESS: COMMUNICATION-CENTRIC ANALYSIS OF COMPLEX EMBEDDED COMPUTING SYSTEMS

Uraz Odyurt, Hugo Meyer, Simon Polstra - *Univ. of Amsterdam* Evangelos Paradas, Ignacio Gonzalez Alonso - *ASML Netherlands B.V.* Andy D. Pimentel - *Univ. of Amsterdam*



Poster Session Time: 15:30-16:00

Session 9A Special Session: CASES: Towards Secure Computer Architecture: Understanding Security Vulnerabilities and Emerging Attacks for Better Defenses <u>Time: 16:00-17:30 | Room: Cavour</u>

Chair:

Sai Manoj Pudukotai Dinakarrao - George Mason Univ.

Organizers:

Sai Manoj Pudukotai Dinakarrao - *George Mason Univ.* Houman Homayoun - *George Mason Univ.*

In the recent years, computer architecture design is primarily driven by security, power, and performance. With the recent evolving attacks on the hardware architectures, design for security is becoming one of the primary constraints to be satisfied. The ever increasing and proliferation of computing devices in different domains ranging from smart homes to defense applications further emphasizes the need for secure computing architecture designs. The recent attacks such as Spectre and Meltdown have exploited the vulnerabilities in the existing architectures. This indicates the need to re-evaluate the existing computer architectures not only in terms of power-performance, but also in terms of security and resilience to such attacks. In order to perform design for security, it is nontrivial to primarily understand the existing attacks and the vulnerabilities in the current computing architectures. In this session, the existing works on hardware security such as Intel's Software Guard Extension (SGX), ARM's TrustZone, and Physically Unclonable Functions (PUFs), will be thoroughly reviewed to understand how the vulnerabilities can be mitigated, which will be introduced in the first talk. Despite many efforts on design for security, there still exist vulnerabilities that can be exploited for crafting the attacks on the hardware. As a case study, we consider one of the recent powerful defenses such as Intel's SGX and show how attacks such as memory corruption can be launched despite having strong defense mechanisms. Towards a lightweight yet powerful defense, the suitability of Hardware Performance Counters (HPCs) for design for security will be discussed in the last talk of the session. HPCs are deployed on the computing architectures for various purposes such as power, performance, and energy management. In the recent days, it has been used for security purposes such as Malware detection. In a similar vein, we discuss the suitability of using the existing HPCs and design of new HPCs for the hardware security. This special session highlights the new challenges and opportunities to design secure computing architectures. The key questions and topics that will be discussed in this session are: How secure are current

Session 9B - CODES+ISSS: Embedded Accelerators Time: 16:00-17:30 | Room: Giolitti

Chair:

Kyoungwoo Lee - Yonsei Univ.

- 9B.1 PAGURUS: LOW-OVERHEAD DYNAMIC INFORMATION FLOW TRACKING ON LOOSELY-COUPLED ACCELERATORS
 - Luca Piccolboni, Giuseppe Di Guglielmo, Luca Carloni Columbia Univ.

9B.2 ARCHITECTURE CONSIDERATIONS FOR STOCHASTIC COMPUTING ACCELERATORS

Vincent T. Lee, Armin Alaghi, Rajesh Pamula, Visvesh S. Sathe, Luis Ceze, Mark Oskin - Univ. of Washington

9B.3 WORK-IN-PROGRESS: AMVP - A HIGH PERFORMANCE VIRTUAL PLATFORM USING PARALLEL SYSTEMC FOR MULTICORE ARM ARCHITECTURES

Jan Henrik Weinstock, Róbert Lajos Bücs, Florian Walbroel, Rainer Leupers, Gerd Ascheid - *Rheinisch-Westfälische Technische Hochschule Aachen*

9B.4 WORK-IN-PROGRESS: FURION: ALLEVIATING OVERHEADS FOR DEEP LEARNING FRAMEWORK ON SINGLE MACHINE

Lihui Jin, Chao Wang, Lei Gong, Chongchong Xu, Yahui Hu, Luchao Tan, Xuehai Zhou - *Univ. of Science and Technology of China*

computing architectures? How are hardware attacks devised based on the current vulnerabilities? How are defenses devised? Are the industrial defense mechanisms really robust? And lastly, does the existing or special type of HPCs be suitable for securing our hardware against attacks such as Spectre, and Meltdown?

9A.1 HARDWARE-ASSISTED SECURITY: FROM TRUST ANCHOR TO MELTDOWN TRUST

Ahmad-Reza Sadeghi - Technische Univ. Darmstadt

9A.2 MEMORY CORRUPTION ATTACKS AGAINST INTEL SGX SHIELDED SOFTWARE

Lucas Davi - Univ. of Duisburg-Essen

9A.3 CAN HARDWARE PERFORMANCE COUNTERS DEFEND ATTACKS SUCH AS MELTDOWN AND SPECTRE?

Houman Homayoun, Sai Manoj Pudukotai Dinakarrao - George Mason Univ.

9A.4 PAPER TITLE - SPECIAL SESSION: ADVANCES AND THROWBACKS IN HARDWARE-ASSISTED SECURITY

Ferdinand Brasser - Technische Univ. Darmstadt Lucas Davi - Univ. of Duisburg-Essen Abhijitt Dhavlle - George Mason Univ. Tommaso Frassetto - Technische Univ. Darmstadt Sai Manoj Pudukotai Dinakarrao, Setareh Rafatirad - George Mason Univ. Ahmad-Reza Sadeghi - Technische Univ. Darmstadt Avesta Sasan, Hossein Sayadi - George Mason Univ. Shaza Zeitouni - Technische Univ. Darmstadt Houman Homayoun - George Mason Univ.

9B.5 WORK-IN-PROGRESS: ON LEVERAGING APPROXIMATIONS FOR EXACT SYSTEM-LEVEL DESIGN SPACE EXPLORATION

Kai Neubauer - Univ. of Rostock Philipp Wanko, Torsten Schaub - Univ. of Potsdam Christian Haubelt - Univ. of Rostock

9B.6 WORK-IN-PROGRESS: A HIGH-BANDWIDTH SNAPPY DECOMPRESSOR IN RECONFIGURABLE LOGIC

Jian Fang, Jianyu Chen - *Delft Univ. of Technology* Harm Peter Hofstee - *IBM Research - Austin* Zaid Al-Ars - *Delft Univ. of Technology* Jan Hidders - *Vrije Univ. Brussels*

9B.7 WORK-IN-PROGRESS: WINONN: OPTIMISING FPGA-BASED NEURAL NETWORK ACCELERATORS USING FAST WINOGRAD ALGORITHM

Xuan Wang, Xuehai Zhou - Univ. of Science and Technology of China



Session 9C - EMSOFT: End-to-End Latency Time: 16:00-17:30 | Room: Einaudi

Chair:

Rüdiger Ehlers - Univ. of Bremen

9C.1 A UNIFIED FRAMEWORK FOR PERIOD AND PRIORITY OPTIMIZATION IN DISTRIBUTED HARD REAL-TIME SYSTEMS

Yecheng Zhao - Virginia Polytechnics and State Univ. Vinit Gala, Haibo Zeng - Virginia Tech

9C.2 IMPROVING AND ESTIMATING THE PRECISION OF BOUNDS ON THE WORST-CASE LATENCY OF TASK CHAINS

Alain Girault - French Institute for Research in Computer Science and Automation

Rafik Henia - Thales Research and Technology

Christophe Prévot, Sophie Quinton - French Institute for Research in Computer Science and Automation

Nicolas Sordon - Thales Research and Technology

9C.3 ANALYTICAL CHARACTERIZATION OF END-TO-END COMMUNICATION DELAYS WITH LOGICAL EXECUTION TIME

Jorge Martinez - Robert Bosch GmbH & Univ. of Modena and Reggio Emilia Ignacio Sañudo, Marko Bertogna - Univ. of Modena and Reggio Emilia

Poster Session Time: 17:30-18:00

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Best Paper Awards Ceremony

Time: 18:00-18:15 | Room: Cavour

Panel - Future of CPS: Here to stay or another fad? Time: 18:15-19:45 | Room: Cavour

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Moderator:

Samarjit Chakraborty - Technical Univ. of Munich

We all know by now that systems with tightly coupled physical and computational elements - where both of them are modeled and analyzed as first class citizens - are referred to as cyber-physical systems (CPS). Developments in CPS over the past 10 years include CPSWeek, a thriving conference dedicated to CPS (ICCPS), an ACM Transactions on CPS, several funding programs both in North America and Europe on CPS, and thousands of research publications on CPS. Many researchers who 10 years ago worked on embedded systems, or control theory, or sensor networks, now claim to be CPS experts. In addition, Computer Scientists in the guise of CPS have now started working on topics like transportation, electricity distribution networks, and building management systems - which previously almost exclusively fell in the domains of civil engineering or power electronics and had apparently no relationship with Computer Science or Computer Engineering.

In spite of these impressive developments, there are several researchers who still believe that CPS is nothing more than another term for embedded systems, or hybrid systems, or sensor networks, that we worked on much before the term CPS became fashionable. This gives rise to several interesting questions:

- Is CPS a research "area"? If so, then is this area defined by a collection of applications? Or did CPS give rise to new theory? There are sessions in ICCPS with papers/talks on three topics that are so disjoint that none of the speakers would understand each other. So what exactly is "CPS" (beyond the definition that we know)?

- If CPS is indeed an area with its own theory and applications, then can we envision a Department of CPS within a university anytime soon?

- How would embedded systems, control theory, sensor networks and other related topics have developed if CPS did not happen? Would we have seen the same results that we have today?

- What is the future of CPS? What should we as researchers do to ensure that CPS has a healthy development in the future? Or will CPS be overtaken by yet another fad?

- What is the opinion of the industry on CPS?

- What is the relationship between CPS and IoT?

The goal of this panel would be to debate on questions like the above, reflect back on how CPS developed and what it holds for the future.

Panelists:

Insup Lee - Univ. of Pennsylvania Giorgio Buttazzo - Scuola Superiore Sant'Anna Chenyang Lu - Washington Univ. Stavros Tripakis - Aalto Univ. Qi Zhu - Northwestern Univ. Frank Mueller - North Carolina State Univ. Dirk Ziegenbein - Robert Bosch GmbH



WORKSHOP SCHEDULE

THURSDAY

EWiLi'18 Thursday, October 4 | Time: 09:00 - 17:30 | Room: Mollino

HENP'18: International Workshop on Highly Efficient Neural Processing *Thursday, October 4 | Time: 09:00 - 17:30 | Room: Giolitti*

INTESA'18 Thursday, October 4 | Time: 09:00 - 17:30 | Room: Sella

THURSDAY & FRIDAY

CyPhy'18: Model-Based Design of Cyber Physical Systems *Thursday, October 4* | *Time: 09:00 - 17:30* | *Room: Sala Stampa*

WESE'18: Embedded and Cyber-Physical Systems Education Thursday, October 4 | Time: 09:00 - 17:30 | Room: Sala Stampa

SYMPOSIA SCHEDULE

THURSDAY & FRIDAY

NOCS 2018: 12th International Symposium on Networks-on-Chip *Thursday, October 4 - Friday, October 5 | Room: Cavour*

RSP Symposium: IEEE International Symposium on Rapid System Prototyping *Thursday, October 4 - Friday, October 5 | Room: Einaudi*



EWiLi 2018

Time: 9:00 - 17:30 | Room: Mollino

Organizers:

Jalik Boukhobza - *Univ. of Western Brittany* Marco Domenico Santambrogio - *Politecnico di Milano* Frank Singhoff - *Univ. of Western Brittany*

EWiLi, the embedded operating system workshop, aims at presenting state-of-theart research, experimentation, significant and original realizations that focus on the design and implementation of embedded operating systems in both academic and industrial worlds.

International Workshop on Highly Efficient Neural Processing (HENP) Time: 9:00 - 17:30 | Room: Giolitti

Organizers:

Yiran Chen - *Duke Univ.,* Sungjoo Yoo - *Seoul National Univ.*

The International Workshop on Highly Efficient Neural Processing is a forum for presentations of state-of-the-art research in highly efficient neural processing. The workshop will combine both oral presentations and posters, which include invited talks from ARM, Google, Facebook, Samsung Electronics, etc.

INTESA Workshop 2018

Time: 9:00 - 17:30 | Room: Sella

The INTESA workshop aims to give an up-to-date picture of intelligent embedded systems architectures and applications with emphasis on Smart IoT and Cyber Physical Systems, including hot topics such as accelerating deep learning. The workshop covers several aspects, from the hardware related ones to embedded software and application issues, being complementary to most of the topic addressed during the ESWEEK. From the market standpoint, scientific progress in this field are considered crucial to fuel a widespread diffusion of the potential benefits offered by the Industry 4.0 perspective. The goal of the event is to create cross-fertilization of ideas between application developers and platform providers with the participation of a mix between academic and industry people.





Model-Based Design of Cyber Physical Systems (CyPhy'18) and Workshop on Embedded and Cyber-Physical Systems Education (WESE'18)

Time: 9:00 - 17:30 | Room: Sala Stampa

CyPhy'18

Cyber physical systems (CPSs) combine computing and networking power with physical components. They enable innovation in a wide range of domains including robotics; smart homes, vehicles, and buildings; medical implants; and future-generation sensor networks. CyPhy'18 brings together researchers and practitioners working on modeling, simulation, and evaluation of CPS, based on a broad interpretation of these areas, to collect and exchange expertise from a diverse set of disciplines. The workshop places particular focus on techniques and components to enable and support virtual prototyping and testing.

General Chair

Walid Taha, Halmstad Univ.

Program Chair

Walid Taha, Halmstad Univ. Martin Törngren, KTH Royal Institute of Technology

WESE'18

The WESE workshop series aims to bring researchers, educators, and industrial representatives together to assess needs and share design, research, and experiences in embedded and cyber-physical systems education. WESE addresses questions such as "What skills and capabilities are required by the engineers of tomorrow", "How should the corresponding educational programs be formed", and "How can effective pedagogic methods be introduced in this domain"?

Chairs

Martin Törngren, KTH Royal Institute of Technology Martin Edin Grimheden, KTH Royal Institute of Technology Falk Salewski, Muenster Univ. of Applied Sciences





NOCS SYMPOSIUM

The International Symposium on Networks-on-Chip (NOCS) Time: 9:00 - 18:00 | Room: Cavour

The International Symposium on Networks-on-Chip (NOCS) is the premier event dedicated to interdisciplinary research on on-chip, chip-scale, and multichip package-scale communication technology, architecture, design methods, applications and systems.

NOCS brings together scientists and engineers working on NoC innovations and applications from inter-related research communities, including computer architecture, networking, circuits and systems, packaging, embedded systems, codesign, and design automation.

2018 General Chairs

Zhonghai Lu, KTH Royal Institute of Technology Sriram Vangal, Intel Corporation

2018 Technical Program Chairs:

Paul Bogdan, Univ. of Southern California Jiang Xu, Hong Kong Univ. of Science and Technology

THURSDAY OCTOBER 4, 2017

[09:00-09:10] Opening Ceremony

[09:10-10:10] Keynote 1

Session chair: Paul Bogdan, Univ. of Southern California Many-Core SoC in Nanoscale CMOS: Challenges & Opportunities Vivek De, Intel Corporation

[10:10 - 10:30] Posters and Coffee Break

[10:30 - 12:35] Regular Paper Session I: Interconnected Multiprocessor Session chair: Jiang Xu, Hong Kong Univ. of Science and Technology

64 - NoC-Based Support of Heterogeneous Cache-Coherence Models for Accelerators

Davide Giri, Paolo Mantovani and Luca Carloni, Columbia Univ.

73 - Exploration of Memory and Cluster Modes in Directory-Based Many-Core CMPs

Subodha Charles, Univ. of Florida, Chetan Arvind Patil, Arizona State Univ., Umit Ogras, Arizona State Univ. and Prabhat Mishra, Univ. of Florida

31 - Accurate Congestion Control for RDMA Transfers

Dimitrios Giannopoulos, Evangelos Mageiropoulos, Nikolaos Chrysos, Giannis Vardas, Leandros Tzanakis and Manolis Katevenis, Foundation for Research and Technoloav Hellas

56 - Testing WiNoC-Enabled Multicore Chips with BIST for Wireless Interconnects

Abhishek Vashist, Amlan Ganguly and Mark Indovina, Rochester Institute of Technology

17 - Towards Energy-efficient High-throughput Photonic NoCs for 2.5D Integrated Systems: A Case for AWGRs

Sebastian Werner, Pouya Fotouhi, Roberto Proietti, Xiao Xian and S.J. Ben Yoo, Univ of California Davis)

[12:35 - 14:00] Lunch

[14:00 - 16:05] Regular Paper Session II: Emerging NoC Architecture and Security

Session chair: Luca Carloni, Columbia Univ.

19 (Best paper candidate) - AxNoC: Low-power Approximate Network-on-**Chips using Critical-Path Isolation**

Akram Ben Ahmed, Keio Univ., Daichi Fujiki, Univ. of Michigan, Hiroki Matsutani, Keio Univ., Michihiro Koibuchi, National Institute of Informatics, Tokyo and Hideharo Amano, Keio Univ.

50 (Best paper candidate) - DAPPER: Data Aware Approximate NoC for **GPGPU** architectures

Venkata Yaswanth Raparti and Sudeep Pasricha, Colorado State Univ.

68 (Best paper candidate) - FreewayNoC: A DDR NoC with Pipeline Bypassing Ahsen Ejaz, Chalmers Univ. of Technology, Vassilios Papaefstathiou, Foundation for

Research & Technology – Hellas and Ioannis Sourdis, Chalmers Univ. of Technology

34 - Brownian Bubble Router: Enabling Deadlock Freedom via Guaranteed Forward Progress

Mayank Parasar, Ankit Sinha and Tushar Krishna, Georgia Institute of Technology

78 - Abetting Planned Obsolescence by Aging 3D Networks-on-Chip Sourav Das, Washington State Univ., Kanad Basu, New York Univ., Jana Doppa,

Washington State Univ., Partha Pratim Pande, Washington State Univ., Ramesh Karri, New York Univ. and Krishnendu Chakrabarty, Duke Univ.

[16:05 - 16:30] Posters and Coffee Break

[16:30 - 17:45] Special Session I: "Securing Networks-on-Chip: A Cross-**Technology Perspective**"

Session chair: Amlan Ganguly, Rochester Institute of Technology Session organizer: Sudeep Pasricha, Colorado State University

Session speakers: Sudeep Pasricha, Colorado State University, Brian Lebiednik, Georgia Institute of Technology, Travis Boraten, Ohio University

1) Travis Boraten: "Securing NoCs against Timing Attacks with Non-Interference Based Adaptive Routing"

2) Sudeep Pasricha: "Hacking Light: Enabling Security in Photonic NoC Architectures"

3) Brian Lebiednik: "Architecting a Secure Wireless Network-on-Chip"

[17:45 - 18:00] Poster Session

57- A Learning-Based Thermal-Sensitive Routing for Power Optimization of **Optical NoCs**

Yaoyao Ye, Zhe Zhang, Renjie Yao, Shanghai Jiao Tong University and Weichen Liu, Nanyang Technological University

59- Approximate Communication for Energy Efficient Networks on Chip

Maurizio Palesi, Davide Patti, Salvatore Monteleone, Giuseppe Ascia, University of Catania, John Jose, IIT Guwahatiand and Vincenzo Catania, University of Catania

45- Improving the Efficiency of Router Bypass

Iván Pérez, Enrique Vallejo and Ramón Beivide, Univ. of Cantabria

62- An Operating System Service for Remote Memory Accesses in Low-Power NoC-Based Manycores

Pedro Henrique Penna, Université Grenoble Alpes, Matheus Souza, Pontifícia Universidade Católica de Minas Gerais, Emmanuel Podestá Junior, Bruno Margues do Nascimento, Márcio Castro, Federal University of Santa Catarina UFSC, François Broquedis, Université Grenoble Alpes, Henrique Freitas, Pontifícia Universidade Católica de Minas Gerais and Jean-François Méhaut, Université Grenoble Alpes

[1900 -] Banquet



NOCS SYMPOSIUM

FRIDAY OCTOBER 5, 2018

[09:00-10:00] Keynote II

Session chair: Jiang Xu, Hong Kong Univ. of Science and Technology

[10:00 - 10:30] Posters and Coffee Break

[10:30 – 11:45] Regular Paper Session III: Cutting-Edge Network-on-Chip Session chair: Jie Han, Univ. of Alberta

21 - A Low-Overhead Multicast Bufferless Router with Reconfigurable Banyan Network

Chaochao Feng, National Univ. of Defense Technology Changsha, Zhuofan Liao, Changsha Univ. of Science & Technology, Zhenyu Zhao, National Univ. of Defense Technology Changsha and Xiaowei He, National Univ. of Defense Technology Chanasha

63 - Critical Packet Prioritisation by Slack-Aware Re-routing in On-Chip Networks

Abhijit Das, Indian Institute of Technology Guwahati, Sarath Babu, Government Engineering College, Idukki, John Jose, Indian Institute of Technology Guwahati, Sangeetha Jose, Government Engineering College, Idukki and Maurizio Palesi, Univ. of Catania

32 - A Diversity Scheme to Enhance the Reliability of Wireless NoC in Multi-Path Channel Environment

Joel Ortiz Sosa, Univ. of Rennes, Olivier Sentieys, Univ. of Rennes and Christian Roland, Université Bretagne Sud

[11:45 - 12:35] Tutorial: "Approximate Computing for Networks on Chip"

Session chair: Paul Bogdan, Univ. of Southern California Session organizers: Dr. Jie Han, Univ. of Alberta and Dr. Eun Jung (EJ) Kim, Texas A&M Univ.

Part I: "Approximate Arithmetic Circuits"

Speaker: Dr. Jie Han, Univ. of Alberta

Part II: "Approximate Networks on Chip"

Speaker: Dr. Eun Jung (EJ) Kim, Texas A&M Univ.

[12:35 - 14:00] Lunch

[14:00 - 15:15] Industrial Session:

Session chair: Zhonghai Lu, *KTH Royal Institute of Technology* 1. Challenges and Opportunities for Edge Cloud architectures

Francesc Guim, Intel Corporation

2. Identifying the gaps between academic research and physical realization of NoCs

Zhiguo Ge, Huawei International Pte Ltd.

3. Co-Design and Abstraction of a Network-on-Chip Using Deterministic Network Calculus

Benoît Dupont de Dinechin, Kalray S.A.

[16:05 - 16:30] Posters and Coffee Break

[16:30 – 17:45] Special Session III: "Realistic Wireless Channel Modelling for Parallel Applications on NoC-based MPSoC"

Session chair: Maurizio Palesi, Univ. of Catania

Session organizers: Jean-Philippe Diguet, *Lab-STICC*, Sujay Deb, *IIIT Delhi*, Sergi Abadal, *Universitat Politècnica de Catalunya*

Session speakers: Jean-Phillipe Diguet, *Lab-STICC*, Sri Harsha Gade, *IIIT Delhi*, Sergi Abadal, *Universitat Politècnica de Catalunya*

1) Jean-Phillipe Diguet: "Accurate Channel Models for Realistic Design Space Exploration of Future Wireless NoCs"

2) Sergi Abadal: "Channel Characterization for Chip-scale Wireless Communications within Computing Packages"

3) Sri Harsha Gade: "On-Chip Wireless Channel Propagation: Impact of Antenna Directionality and Placement on Channel"

[17:45 - 18:00] Closing Remark with Best Paper Announcement





RSP SYMPOSIUM

The International Symposium on Rapid System Prototyping (RSP) Time: 8:30 - 17:00 | Room:

The International Symposium on Rapid System Prototyping (RSP) emphasizes design experience sharing and collaborative approach between hardware and software research communities from industry and academy. It considers prototyping as an iterative design approach for embedded hardware and software systems. The RSP series of symposium aim at bridging the gaps in embedded system design between applications, architectures, tools, and technologies to achieve rapid system prototyping of emerging software and hardware systems.

THURSDAY OCTOBER 4, 2018

[09:00-09:10] Opening Ceremony

[09:10-10:10] Keynote 1

Many-Core SoC in Nanoscale CMOS: Challenges & Opportunities Vivek De, *Intel Corporation* In combination with NOCS 2018

[10:10 - 10:30] Coffee Break

[10:30 – 10:55] Synthesis of Full Hardware Implementation of RTOS-Based Systems

Yuuki Oosako, Kwansei Gakuin Univ., Nagisa Ishiura, Kwansei Gakuin Univ., Hiroyuki Tomiyama, Ritsumeikan Univ. and Hiroyuki Kanbara, ASTEM RI Kyoto

[10:55 – 11:20] Accurate MPSoC prototyping platform and methodology for the studying of the Linux synchronization barrier slowdowns issues

Maxime France-Pillois, Univ. Grenoble Alpes Jérôme Martin, Univ. Grenoble Alpes and Frédéric Rousseau, Univ. Grenoble Alpes

[11:20 – 11:45] Estimating the Impact of Architectural and Software Design Choices on Dynamic Allocation of Heterogeneous Memories

Tristan Delizy, Univ Lyon, INSA Lyon, Inria, CITI, Stephane Gros, eVaderis, Kevin Marquet, Univ Lyon, INSA Lyon, Inria, CITI, Matthieu Moy, Univ. Lyon, Univ. Lyon 1, Inria, CNRS, ENS de Lyon, LIP, Tanguy Risset, Univ. Lyon, INSA Lyon, Inria, CITI and Guillaume Salagnac, Univ Lyon, INSA Lyon, Inria, CITI

[11:45 – 12:10] A Comprehensive Fault Injection Strategy for Embedded Systems Reliability Assessment

Alexandre Chabot, Ihsen Alouani, Smail Niar and Réda Nouacer

[12:10 - 12:35] [TBD] Constraint Specification Language (CSL) use in the test program generator

Bernhard Egger, Seoul National Univ.

[10:55 - 11:20] Lunch

[14:00 – 14:25] Rapid Prototyping of Parameterized Rotated and Cyclic Q Delayed Constellations Demapper

Muhammad Waqas, Atif Jafri, Amer Baghdadi and M. Najam Islam

[14:25 - 14:50] Assessment of a BeagleBone Black High Sampling Rate Digital Waveform Generator

Kevin Verniers, Liesbet Van der Perre and Nobby Stevens, KU Leuven, ESAT-DRAMCO, Ghent Technology Campus

[14:50 – 15:15] Semantics-directed Prototyping of Hardware Runtime Monitors

William Harrison, Univ. of Missouri and Gerard Allwein, US Naval Research Laboratory

[15:15 – 15:40] [TBD] a prototype platform for energy harvesting powered embedded system with non-volatile processor

Jingtong Hu, Univ. of Pittsburgh

[15:40 - 16:05] Message-oriented Devices on FPGAs

Thomas Baumela, Olivier Gruber, Muller Olivier and Frédéric Pétrot

[16:05 - 16:30] Coffee Break

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Frédéric Rousseau, *TIMA* Sungjoo Yoo, *Seoul National Univ.*

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Session 3

[16:30-16:55] [TBD]

Nicola Bombieri, Universita` di Verona

[16:55 – 17:20] PyXEL: An Integrated Environment for the analysis of Fault Effects in SRAM-based FPGA Routing

Cinzia Bernardeschi, Univ. di Pisa

[17:20 - 17:45] viciLogic2.0: Online digital systems training and prototyping using PYNQ SoC

Fearghal Morgan, National Univ. of Ireland, Declan O'Loughlin, National Univ. of Ireland, Jeremy Audiger, National Univ. of Ireland, Yohan Boyer, National Univ. of Ireland, Niall Timlin-Canning, National Univ. of Ireland, Krzysztof Kępa, National Univ. of Ireland, Ian Gallivan, National Univ. of Ireland, Frank Callaly, National Univ. of Ireland, László Bakó, Sapientia Hungarian Univ. of Transylvania

FRIDAY OCTOBER 5, 2018

[09:00 – 10:00] Keynote II - NoCs: a short history of success and a long future

Giovanni De Micheli, *EPF Lausanne* In combination with NOCS 2018

[10:10 - 10:30] Coffee Break

Session 3

[10:30 – 10:55] Ambient Intelligence for the Internet of Things through Context-Awareness

Rodrigo Meurer, Federal Univ. of Santa Catarina, Antonio Frohlich, Federal Univ. of Santa Catarina and Jomi Hübner, Federal Univ. of Santa Catarina

[10:55 – 11:20] Towards Trainable Synthesis for Optimized Circuit Deployment on FPGA

Jean-Philippe Legault, Panagiotis Patros and Kenneth Kent, Univ. of New Brunswick

[11:20 – 11:45] Resilience Evaluation for Approximating SystemC Designs Using Machine Learning Techniques

Mehran Goli, Univ. of Bremen, Jannis Stoppe, Univ. of Bremen and Rolf Drechsler, Univ. of Bremen and Cyber-Physical Systems, DFKI GmbH

[11:45 – 12:10] FPGA Prototyping of Low-Precision Zero-Skipping Accelerator for Neural Networks

Dongyoung Kim, Soobeom Kim and Sungjoo Yoo, Seoul National Univ.

[12:10 - 12:35] Lunch & End



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