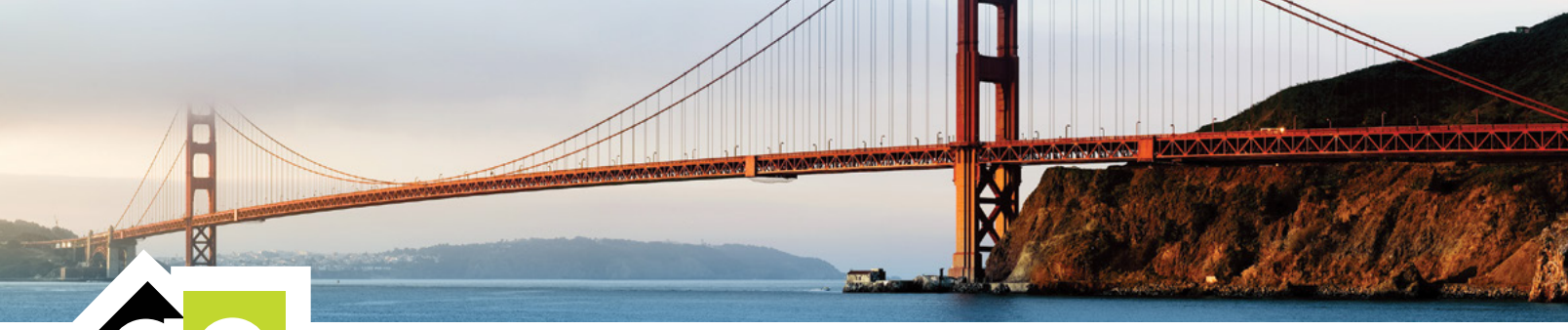

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DESIGN AUTOMATION CONFERENCE

FROM CHIPS TO SYSTEMS – LEARN TODAY, CREATE TOMORROW

CONFERENCE PROGRAM & EXHIBITS GUIDE

JUNE 24-28, 2018 | SAN FRANCISCO, CA | MOSCONE CENTER WEST

FROM CHIPS TO SYSTEMS – LEARN TODAY, CREATE TOMORROW

Sponsored by: SIGDA, Electronic System Design Alliance, CEDA

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GENERAL CHAIR'S WELCOME

Dear Colleagues,

Welcome to the 55th Design Automation Conference!

It is great to have you join us in San Francisco, one of the most beautiful cities in the world and now an information technology capital (it's also the city that my son is named after). A lot is waiting for you on the three floors of the splendid Moscone West Conference Center.

After 54 years, DAC continues to be the premier conference for **design and design automation for IC chips all the way to systems**, and this year it's filled with new energy. With the help of countless volunteers, the DAC executive committee has assembled a top-tier research program, highly-regarded practitioners' forums, and widely-represented exhibition. I briefly highlight some programs below. Many more are for you to explore.

AI/machine learning is the new featured topic area at #55DAC. You will hear keynotes, invited talks, tutorials and research paper presentations (close to 20 sessions altogether) on innovative hardware, software and system designs of neural network accelerators as well as the application of AI/machine learning techniques to advancing EDA. You will also hear from the winners of DAC's first **System Design Contest**, in which more than 100 teams competed in developing low-energy and high-performance implementations of neural network-based object detection for drones and will get to see demos of the winning entries on the exhibit floor in the **Smart Systems Square**.

Besides 50 sessions related to core **EDA** and **IP** topic areas, #55DAC features:

- 23 sessions in **Design** (from heterogeneous SoCs, architectures, circuits, to emerging technologies)
- 12 (six system, six auto) sessions in **Embedded Software and Systems and Auto** (from IoT, CPS, embedded memory, to autonomous driving)
- 16 sessions in **Security/Privacy** (from secure processor design, IC reverse engineering, hands-on IoT hacking, to blockchain for security), including presentations by winners of the Hack@DAC contest and hands-on IoT hacking demos in DAC Pavlion;
- 5 sessions in **IoT** (from embedded machine learning, IoT security, runtime support, to industrial IoT architectures)

As always, you will find much action and excitement on the exhibition floor. To be more precise, the "exhibition floor" this year actually occupies two floors physically. With our twice daily coffee breaks on the exhibition floor, you will be able to visit over 175 exhibitors and our popular DAC Pavilion. #55DAC's exhibition halls bring attendees several new areas/activities:

- **Design Infrastructure Alley** is for professionals who manage the HW and SW products and services required by design teams. It houses a dedicated **Design-on-Cloud Pavilion** featuring presentations from the Design Infrastructure Alley exhibitors and invited companies.
- **Smart Systems Square** is a centralized exhibit pavilion where engineers can interact with developers, network and platform providers, and verification experts for AI and machine learning applications. It also showcases live demos of the winning entries from the System Design Contest.

Like to have some hands-on fun with building a mini robot? Take the Sunday Sumo Robot Class to learn all that is needed to get your robot ready for the Sumo Robot Competition at 6:00 p.m. during the Tuesday night reception. Do not have time to manage your own? Come and see Sumo robot teams performing pre-competition practices in the **Smart Systems Square** in preparation for their competition.

The DAC Silicon/Technology Art Show is back in full force. One cannot find a better place than San Francisco to have this! The Art Show will highlight the beauty of electronic design and algorithms and showcase the works of companies and individuals that contribute to our industry. I encourage you to attend the Art Show/evening reception on Monday starting at 6:00 p.m.

Do you worry about missing any events that you want to attend? Download DAC's mobile app! It not only makes it easier for you to manage your schedule and activities at the show but also navigate the three floors of Moscone West.

I hope I will get to talk to many of you in person during the week of #55DAC. Together, we LEARN TODAY and CREATE TOMORROW.

Enjoy the #55DAC!

X. Sharon Hu

TABLE OF CONTENTS

ACM/SIGDA

IEEE/COUNCIL ON ELECTRONIC DESIGN AUTOMATION

ELECTRONIC SYSTEM DESIGN ALLIANCE

CONFERENCE INFORMATION

EXHIBIT HOURS

LOCATION: EXHIBIT HALLS LEVEL 1 & 2

Monday, June 25	10:00am - 6:00pm
Tuesday, June 26	10:00am - 6:00pm
Wednesday, June 27	10:00am - 6:00pm

REGISTRATION HOURS

LOCATION: MOSCONE CENTER WEST – LEVEL ONE LOBBY

Friday, June 22	12:00pm – 6:00pm
Saturday, June 23 - Sunday, June 24	8:00am – 6:00pm
Monday, June 25 - Wednesday, June 27	7:00am – 7:00pm
Thursday, June 28	7:00am – 5:00pm

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STAY CONNECTED

WIRELESS INTERNET

Moscone Center West has complimentary wireless internet service throughout the facility.

"BIRDS-OF-A-FEATHER" MEETINGS

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF).

All BOF meetings are held at the Moscone Center West, Tuesday June 26 from 7:00 - 8:30pm.

To arrange a BOF Meeting, please email Trevor Kearns at trevor@dac.com

FIRST AID ROOM

First Aid Room is located on Level 1 of Moscone Center West.

First Aid Room Hours:
Friday, June 22 & Saturday, June 23: 8:00am - 5:00pm.
Sunday, June 24: 8:00am - 10:30pm,

Monday, June 25 & Tuesday, June 26: 8:00am - 7:00pm,
Wednesday, June 27: 8:00am - 10:00pm,
Thursday, June 28: 8:00am - 5:00pm.

In-house security: x511 on a white house phone or on a cell phone, dial (415) 974-4021

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DAC NETWORKING OPPORTUNITIES

WELCOME RECEPTION & HOT 55: DAC KICK-OFF PARTY

Sunday, June 24
6:00 - 10:00pm | Level 3 Lobby
Join fellow attendees for the first event to network and kick-off DAC 2018

NETWORKING RECEPTION AND SILICON/TECHNOLOGY ART SHOW

Monday, June 25
6:00 - 7:00pm | Level 2 Lobby
Join attendees for refreshments and lively discussion and DAC's 2nd Silicon/Technology Art Show.

The Silicon/Technology Art Show will feature stunning images submitted by DAC attendees that demonstrate the beauty of everyday work in this industry. Submitted pieces will be judged in various categories and the winners for each category will be announced during the reception.

Awards include:

Most Insightful

Most Inspiring

Grand Prize

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AMIQ

NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Tuesday, June 26
6:00 - 7:00pm | Level 2 Lobby
Join us in the Level 2 Lobby to see Work-in-Progress posters and enjoy light hors d'oeuvres and beverages.

Thank You to Our Reception Sponsor

AMIQ

NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Wednesday, June 27
6:00 - 7:00pm | Level 2 Lobby
Join us in the Level 2 Lobby to see Work-in-Progress posters and enjoy light hors d'oeuvres and beverages.

KEYNOTE PRESENTATIONS

KEYNOTE: LIVING PRODUCTS: BUILDING CONNECTED DEVICES THAT LEARN AND EVOLVE

SARAH COOPER – *GM of IoT Solutions, Amazon Web Services, Inc., Mountain View, CA*

Monday, June 25 || 9:20 – 10:00am || Room 3008

It took powerful hardware platforms to enable the ecosystem that turned mobile phones from communication devices to personal assistants, shopping portals, gaming consoles, and so much more. Connected products need a similar transformation from individual actors performing essentially the same function just better to an interconnected backdrop of data driving dynamic device collaboration proactively building consumer experiences, i.e. ambient intelligence. Are recent advancements in embedded AI, security, remote management and end-to-end tools enough to drive ambient intelligence or do we need more?

See page 20 for more details.

KEYNOTE: THE FUTURE OF COMPUTING: PUSHING THE LIMITS OF PHYSICS, ARCHITECTURES & SYSTEMS FOR AI

DARIO GIL – *Vice President of AI and IBM Q, IBM Research, Yorktown Heights, NY*

Tuesday, June 26 || 9:20 – 10:00am || Room 3008

The extraordinary progress in AI over the last few years has been enabled, in part, by modern advancements in computing. Algorithmic ideas that had been around for decades have finally been brought to life thanks to Moore's Law and innovations in microprocessor and computing architectures. As Moore's Law slows and data volumes explode we can expect to see new types of innovations emerge that will allow the rate of progress to continue. My presentation will cover state-of-the art computing for AI, as it exists today, as well as a roadmap of innovations that will lead us into the decade(s) to come. This includes the importance of approximate computing (both algorithms and hardware), analog devices for AI, and quantum computing for AI. I will also highlight how these innovations bring forth both challenges and unique opportunities for the design automation community.

See page 33 for more details.

KEYNOTE: A NEW GOLDEN AGE FOR COMPUTER ARCHITECTURE: DOMAIN SPECIFIC ACCELERATORS AND OPEN RISC-V

DAVID A. PATTERSON – *Distinguished Softawre Engineer, Google, Inc. & Professor Emeritus, Univ. of California, Berkeley, Mountain View, CA*

Wednesday, June 27 || 9:20 – 10:00am || Room 3008

The 1980s enjoyed architectural innovation when high-level language programming surpassed assembly language programming, which made instruction set innovation plausible, and because the Mead-Conway democratized chip design. Innovations like RISC, VLIW, and superscalar doubled performance every 18 months. The following decades saw consolidation, leveraging Moore's Law via higher clock rates and larger caches.

The ending of Moore's Law brought performance to a standstill. Processors improved only 3% last year, taking 20 years to double! Moreover, the new Spectre security enables timing attacks that leak information at ≥10 kilobits/second.

The only likely path left is changes in the instruction set architecture (ISA). For example, Domain Specific Accelerators (DSAs) can perform narrow tasks an order of magnitude more efficiently. For proprietary ISAs, we must wait years for improved chips.

The RISC-V ISA opens another path. The plasticity of FPGAs and free implementations of RISC-V enable experimental investigations of novel architectures deployed and iterated in days. FPGAs are slow but fast enough to run trillions of instructions or be deployed to test against real attacks.

Unlike proprietary ISAs, everyone can help. For tall challenges like these, we want all the best minds working on them.

We give examples of DSA chips that deliver tenfold improvements in performance-energy and sketch an example of improving RISC-V security by defeating Return Oriented Programming.

RISC-V's openness and flexibility can meet the cost-performance-energy-security demands of the Post Moore's Law era. Freeing architects from the chains of proprietary ISAs may well lead to another Golden Age for computer architecture.

See page 54 for more details.

KEYNOTE: AUTOMATION VS. AUGMENTATION: SOCIALLY ASSISTIVE ROBOTICS AND THE FUTURE OF WORK

MAJA MATARIĆ – *Professor and Chan Soon-Shiong Chair of Computer Science, Neuroscience, and Pediatrics, Univ. of Southern California, Los Angeles, CA*

Thursday, June 28 || 9:20 – 10:00am || Room 3008

Robotics is booming all around us. A field that was originally driven by the desire to automate physical work is now raising concerns about the future of work. Less discussed but no more important are the implications on human health, as the science on longevity and resilience indicates that having the drive to work is key for health and wellness. However, robots, machines that were originally invented to automate work, are also becoming helpful by not doing any physical work at all, but instead by motivating and coaching us to do our own work, based on evidence from neuroscience and behavioral science demonstrating that human behavior is most strongly influenced by physically embodied social agents, including robots.The field of socially assistive robotics (SAR) focuses on developing intelligent socially interactive machine that that provide assistance through social rather than physical means. The robot's physical embodiment is at the heart of SAR's effectiveness, as it leverages the inherently human tendency to engage with lifelike (but not necessarily human-like or otherwise biomimetic) agents. People readily ascribe intention, personality, and emotion to robots; SAR leverages this engagement to develop robots capable of monitoring, motivating, and sustaining user activities and improving human learning, training, performance and health outcomes. Human-robot interaction (HRI) for SAR is a growing multifaceted research field at the intersection of engineering, health sciences, neuroscience, social, and cognitive sciences, with rapidly growing commercial spinouts. This talk will describe research into embodiment, modeling and steering social dynamics, and long-term adaptation and learning for SAR, grounded in projects involving multi-modal activity data, modeling personality and engagement, formalizing social use of space and non-verbal communication, and personalizing the interaction with the user over a period of months, among others. SAR systems have been validated with a variety of user populations, including stroke patients, children with autism spectrum disorders, elderly with Alzheimer's and other forms of dementia; this talk will cover the short, middle, and long-term commercial applications of SAR, as well as the frontiers of SAR research.

See page 75 for more details.

VISIONARY & SKY TALKS

SKY TALK: AUTOMATING INTELLIGENCE: MACHINE LEARNING AND THE FUTURE OF MANUFACTURING

Anna-Katrina Shedletsky – *CEO and Founder, Instrumental, Inc., Los Altos, CA*

Monday, June 25 || 1:00 – 1:25pm || DAC Pavilion – Booth 2161

Biography: Anna-Katrina Shedletsky is the CEO and founder of Instrumental, a manufacturing data company that uses machine learning to find anomalies on consumer electronics assembly lines. She has two degrees in mechanical engineering from Stanford University, and went on to work as a Product Design Engineer at Apple. During her six years there, she designed mechanical components for three iPods and led system product design for the Apple Watch Series 1. After spending over 300 days in China finding and fixing issues on manufacturing lines, she started Instrumental to build an intelligent quality system to modernize manufacturing. Instrumental customers range from startups to Fortune 500s and span consumer electronics, apparel, and more.

See page 22 for more details.

SKY TALK: DARPA IS BUILDING A SILICON COMPILER

Andreas Olofsson – *Defense Advanced Research Projects Agency, Arlington, VA*

Tuesday, June 26 || 1:00 – 1:25pm || DAC Pavilion – Booth 2161

Biography: Mr. Andreas Olofsson joined DARPA as a program manager in the Microsystems Technology Office in January 2017. His interests include intelligent design automation, system optimization, and open hardware. Prior to his arrival at DARPA, Mr. Olofsson devoted 20 years to designing and testing low-power processors and mixed-signal circuits at Texas Instruments, Analog Devices, and Adapteva. Chip products designed by Mr. Olofsson include low-power digital signal processors (DSPs), charge-coupled device (CCD) readout circuits, and massively parallel reduced instruction set computing (RISC) processors. From 2008 to 2016, Mr. Olofsson served as the CEO of Adapteva, where he developed the Epiphany architecture and Parallella open source computer. The Parallella democratized access to parallel computing and catalyzed the growth of a community of 10,000 developers and 200 universities across the globe. Mr. Olofsson received his Bachelor of Science in Physics and Electrical Engineering and Master of Science in Electrical Engineering from the University of Pennsylvania. Mr. Olofsson is a member of IEEE and holds nine U.S. patents.

See page 39 for more details.

VISIONARY TALK: CHALLENGES TO ENABLE 5G SYSTEM SCALING

PR "Chidi" Chidambaram – *Vice President, Engineering Qualcomm, Inc., San Diego, CA*

Wednesday, June 27 || 9:00 – 9:20am || Room 3008

Biography: Chidi Chidambaram leads the process technology and foundry engineering team at Qualcomm as Vice President Engineering. Chidi's team has enabled Qualcomm to lead the fab less industry bringing leading edge semiconductor technologies to manufacturing - Qualcomm was the first company to ship large volume products in 10 nm technology in 2017. Chidi's team is also enabling the transition of RF devices to 3D and SOI transistors. Chidi was very instrumental in creating a multi sourcing strategy for silicon wafers that was key to Qualcomm growing to be the leading cell phone chip supplier yet staying fabless. Earlier Chidi developed silicon technology at Texas Instruments and was instrumental in the first embedded SiGe implementation at TI; for which, he was recognized with the Andretti award. Chidi's 20+ year semiconductor career has evenly straddled research and development with over 60 each of refereed articles and patents.

See page 54 for more details.

Claude Moughanni | 1960 - 2018

Claude Moughanni was a leader in the DAC organization, having served as the IP Track Chair from 2016 to 2018. Through his tireless efforts, Claude helped build up the IP Track into a fixture at the conference. As he had done many times in his professional career, Claude built up a strong team that is committed to continuing to enhance the IP Track and DAC as a whole.

During his 30+ year career, Claude Moughanni excelled in the design of products as varied as gate arrays, standard cells, cache and memory management subsystems, content addressable memories, phase locked loops, and low-power microprocessors. He managed global and multi-disciplinary teams developing products such as Digital Car Radios, microprocessors, Process Design Kits and digital libraries. Claude worked for many years at Freescale (and Motorola before that), and most recently, Claude was a key member of the CTO Office at Lattice Semiconductor. He was granted 19 patents, and held a Bachelor's degree in Electrical Engineering from the Catholic University of America and a Master's degree in Electrical and Computer Engineering from Carnegie-Mellon University.

Claude Moughanni was an adored family man who relished time spent with his loved ones. He delighted in refining and cultivating his lifelong passion for photography. Claude is survived by his wife Rhina, son Hiram and his wife Jennifer and their children Ari and Nadine, and his daughter Samia.

2018 AWARDS

The 55th DAC will recognize success and excellence for the following individuals in the field of design automation of electronic systems.

2017 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO ELECTRONIC SYSTEM DESIGN

Dr. Rob A. Rutenbar, Senior Vice Chancellor for Research at the University of Pittsburgh

Dr. Rutenbar is being honored for his contributions to analog design automation and impact on EDA education. As an academic, he developed a wide range of fundamental models, algorithms and tools for analog IC designs. As an entrepreneur, he co-founded Neolinear, one of the most successful analog tool companies, to bring his research efforts to a larger design community. (Neolinear was acquired by Cadence in 2001.)

A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Dr. Hans Eisenmann, PDF Solutions GmbH, Formerly Technische Universität München; The Late Frank M. Johannes, Formerly Technische Universität München.

Sponsored by the IEEE Council on Electronic Design Automation and the ACM Special Interest Group on Design Automation. For seminal contributions to VLSI placement impacting academia and industrial practices.

Hans Eisenmann and Frank M. Johannes, "Generic Global Placement and Floorplanning" Proc. of the 35th Design Automation Conference, pp. 269 – 274, June 1998.

2018 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

Anne Cirkel, Senior Director for Technology Marketing at Mentor, a Siemens Business

This annual award, named for Marie R. Pistilli, the former organizer of DAC, recognizes individuals who have visibly helped advance women in Electronic Design.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIP FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

Myles Cherebin

The objective of the P.O. Pistilli Undergraduate Scholarship for Advancement in Computer Science and Engineering is to increase the pool of professionals in Electrical and Computer Engineering and Computer Science from under-represented groups (female, African-American, Hispanic, Native American, and disabled students). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. DAC funds a $4,000 scholarship, renewable up to five years, to graduating high school seniors who have a 3.00 GPA or better (on a 4.00 scale).

DAC UNDER-40 INNOVATORS AWARD

The Under-40 Innovators Award is sponsored by Association for Computing Machinery (ACM), the Electronic Systems Design Alliance (ESDA), and the Institute of Electrical and Electronics Engineers (IEEE). The award will recognize the top five young innovators (nominees should be 40 years or younger in age as of June 1, 2018) who are movers and shakers in the field of design and automation of electronics.

SYSTEM DESIGN CONTEST WINNERS

HACK@DAC WINNERS

IEEE CEDA OUTSTANDING SERVICE AWARD

Michael 'Mac' McNamara, Adapt-IP

For outstanding service to the EDA community as DAC General Chair in 2017.

Vijaykrishnan Narayanan, Pennsylvania State University

For his outstanding 4-year service as Editor-in-Chief (EiC) for the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).

IEEE FELLOW

Yiran Chen, Duke University

For contributions to spintronic memory.

IEEE FELLOW

Zhuo Li, Cadence Design Systems, Inc.

For contributions to physical synthesis and modeling of integrated circuits.

IEEE FELLOW

Sanjit A. Seshia, University of California, Berkeley

For contributions to formal methods for inductive synthesis and algorithmic verification.

IEEE FELLOW

Mark M. Tehranipoor, University of Florida

For contributions to integrated circuits security and trust.

IEEE FELLOW

Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg

For contributions to hardware/software co-design for embedded systems.

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

Luca Amarú, Pierre-Emmanuel Gaillardon, Giovanni De Micheli

Majority-Inverter Graph: A New Paradigm for Logic Optimization," Vol. 35, Issue 5, pp. 806 – 819, May 2016.

ACM SIGDA PIONEER AWARD

Mary Jane Irwin - *Pennsylvania State University*

For contributions to VLSI architectures, electronic design automation and community membership.

2018 ACM TODAES BEST PAPER AWARD

Kan Xiao, Domenic Forte, Yier Jin, Ramesh Karri, Swarup Bhunia, Mark M. Tehranipoor

"Hardware Trojans: Lessons Learned after One Decade of Research," ACM TODAES Volume 22 Issue 1, December 2016, Article No. 6.

ACM SIGDA DISTINGUISHED SERVICE AWARD

Chuck Alpert, Cadence Design Systems

For significant contributions to DAC.

Jörg Henkel, Karlsruhe Institute of Technology

For leading SIGDA efforts in Europe and DATE.

Michael 'Mac' McNamara, Adapt-IP

For sustained contributions to the design automation community and DAC.

Michelle Clancy, Cayenne Communication

For sustained contributions to the community, especially DAC.

ACM SIGDA OUTSTANDING NEW FACULTY AWARD

Shimeng Yu, Arizona State University

ACM SIGDA OUTSTANDING PH.D. DISSERTATION AWARD

Xiaoqing Xu – "Standard Cell Optimization and Physical Design in Advanced Technology Nodes"

Advisor: David Pan

Pramod Subramanyan – "Deriving Abstractions to Address Hardware Platform Security Challenges"

Advisor: Sharad Malik

ACM FELLOW

Martin Wong - *University of Illinois Urbana-Champaign*

For contributions to the algorithmic aspects of electronic design automation (EDA).

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IMPACT OF AI AND DEEP LEARNING ON SEMICONDUCTOR MARKET OPPORTUNITIES FOR DESIGNS

Date: Monday, June 25 || Time: 10:30 - 11:00am || Room: DAC Pavilion - Booth 2161
Keywords: Emerging Architectures & Technologies || Topic Area: Machine Learning/AI

AI will be disruptive to many application segments, but with many growth opportunities for new semiconductor products, but where new approaches to designs are required because of the complexity of the applications that need to be supported. The emergence and adoption of 5G will provide the high bandwidth and low latency required for autonomous driving as well as the ability to support tens of billions of IoT devices. Many new applications and services will emerge because of the bandwidth provided by 5G.

The migration to ≤10nm will require the development of ultra-high throughput processors along with the supporting algorithms. The cost of designing these processors will be hundreds of millions of dollars, and the result is that with the present approaches to designs, the number of new products will be small. Approaches are needed in order to increase the efficiency of designs, and new business models are also needed to obtain higher payback from the design.

There will also be an increasing number of designs in 28nm and derivatives where RF and eNVM functionality will be mainstream. There will also be increased adoption of multichip packaging which will also require continued enhancements in design implementation technologies. The breadth of applications that will need to be supported will increase, and a key limitation will be shortages of design engineers.

It is clear that the value of high-level design expertise will increase significantly during the next decade, but a critical need is also to use AI and computer power to increase the productivity of the design engineers.

SPEAKER:

Handel Jones - *IBS, Inc., Los Gatos, CA*

STRAIGHT TALK WITH WALLY RHINES, PRESIDENT AND CEO OF MENTOR, A SIEMENS BUSINESS

Date: Monday, June 25 || Time: 11:30am - 12:15pm || Room: DAC Pavilion - Booth 2161
Keywords: Emerging Architectures & Technologies, Architecture & System Design
Topic Area: Machine Learning/AI, IoT

MODERATOR:

Ed Sperling - *SemiEngineering Magazine, San Jose, CA*

Wally Rhines, President and CEO of Mentor, a Siemens Business, sits down with Semiconductor Engineering's Ed Sperling to discuss the big shifts in technology, from AI to autonomous cars to the growth of the Internet of Things and the Industrial Internet of Things. What kinds of shifts can we expect to see in the future, who's going to be best positioned to take advantage of them, and what will the semiconductor industry look like in five years as these changes begin taking hold? Who will be the winners and who will be the losers?

SPEAKER:

Wally Rhines - *Mentor, A Siemens Business, Wilsonville, OR*

DESIGN FOR SAFETY AND RELIABILITY - ADAS AND AUTONOMOUS VEHICLE SOCS

Date: Monday, June 25 || Time: 2:15 - 2:45pm || Room: DAC Pavilion - Booth 2161
Keywords: Emerging Architectures & Technologies || Topic Area: Automotive, Design

ORGANIZER:

Ravi Ravikumar - *NetSpeed Systems, San Jose, CA*

The transformation that automobiles are going through with ADAS (advanced driver assistance systems) and autonomous vehicle systems in just the last 3 to 4 years is so radical compared to what happened to the vehicle technology in the last 50 years. It is simply not an option for an autonomous vehicle system to abruptly relinquish control and expect a human driver to safely take over, thereby driving the stakes for safety sky-high. The buck stops with the system on chip (SoC) that orchestrates the autonomous driving capability of the vehicle, forcing the need to bring in a variety of data types from a camera, lidar, and radar requires a heterogeneous set of processing elements on-chip. To quickly and accurately process the data and take actions that ensure safety for everyone involved safety and reliability have to be designed in.

SPEAKERS:

Sundari Mitra - *NetSpeed Systems, San Jose, CA*
Hideki Sugimoto - *NSITEXE, Inc., Tokyo, Japan*

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HOW CLOSE TO THRESHOLD-VOLTAGE DESIGN CAN WE GO WITHOUT GETTING OUR FINGERS BURNT?

Date: Monday, June 25 || Time: 3:00 - 3:45pm || Room: DAC Pavilion - Booth 2161
Keywords: Low-Power & Reliability, Emerging Architectures & Technologies
Topic Area: Design, IoT

MODERATOR:

Brian Fuller - *Arm, Ltd., San Jose, CA*

ORGANIZER:

Jan Willis - *Calibra Consulting, Menlo Park, CA*

Energy consumption is the driving design parameter for many systems that must meet "always-on" market requirements and in IoT in general. For decades, the semiconductor industry has attempted to leverage the essential principle that lowering voltage is the quickest, biggest way to reduce energy for a SoC. Some today contend sub-threshold voltage design is viable while others argue for near-threshold voltage design as the minimum. This panel will explore how far below nominal voltage we can design, in what applications it makes sense and in what ways it will cost us.

PANELISTS:

Scott Hanson - *Ambiq Micro, Austin, TX*
Mahbub Rashed - *GLOBALFOUNDRIES, San Jose, CA*
Lauri Koskinen - *Minima Processor Oy, Espoo, Finland*
Paul Wells - *sureCore Ltd., Sheffield, United Kingdom*

YOUNG UNDER 40 INNOVATORS AWARD PANEL

Date: Monday, June 25 || Time: 4:30 - 5:00pm || Room: DAC Pavilion - Booth 2161
Keywords: Any || Topic Area: Design

MODERATOR:

Junko Yoshida - *EE Times, San Francisco, CA*

ORGANIZER:

Michelle Clancy - *Cayenne Communication, Sunnyvale, CA*

Please join a lively discussion with the recipients of the 2018 Young Under 40 Innovator Award. Winners of the award will be announced on Monday, June 25 during the opening session.

THE STATE OF EDA: A VIEW FROM WALL STREET

Date: Tuesday, June 26 || Time: 10:30 - 11:00am || Room: DAC Pavilion - Booth 2161
Keywords: Any, Emerging Architectures & Technologies, Any || Topic Area: EDA, Design

We will examine the financial performance and structure of the EDA industry from 2007 through 2017, as well as some of the technical trends and requirements that have affected its performance and the EDA companies' strategies. In addition, we will examine the effects in recent years of semiconductor industry consolidation, including in particular the progression of semiconductor R&D spending. Lastly, we will examine how the market value of the publicly-held EDA companies has evolved and provided our financial projections for EDA through 2020.

SPEAKERS:

Jay Vleeschhouwer - *Griffin Securities, Inc., New York, NY*

STRAIGHT TALK WITH LIP-BU TAN, CEO, CADENCE DESIGN SYSTEMS

Date: Tuesday, June 26 || Time: 11:30am - 12:15pm || Room: DAC Pavilion - Booth 2161
Keywords: Emerging Architectures & Technologies || Topic Area: EDA, Design

MODERATOR:

Ed Sperling - SemiEngineering Magazine, San Jose, CA

Cadence's CEO talks with Semiconductor Engineering's Ed Sperling about the expanding role of data in our economy and how the dominant waves of technology, including mobile, edge computing, cloud, and automotive, are all being transformed by machine learning and AI. This talk will focus on what this means for EDA, the semiconductor ecosystem, and business as a whole, including the opportunities and threats ahead as we transition to a data-driven economy.

SPEAKERS:

Lip-Bu Tan - *Cadence Design Systems, Inc., San Jose, CA*

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CAN WE USE BLOCKCHAIN TO SECURE EVERYTHING? SHOULD WE?

Date: Tuesday, June 26 || Time: 2:15 - 2:45pm || Room: DAC Pavilion - Booth 2161
Keywords: Emerging Architectures & Technologies || Topic Area: Security/Privacy, IoT

MODERATOR:

James Hogan - *Vista Ventures, Santa Cruz, CA*

The cost of cybersecurity & data breaches soars, approaching $4B/year. More importantly, these breaches are tearing apart traditional business and political interactions like credit checks and campaign emails, and they have eroded trust in machine-to-machine interactions.

But blockchain technology – which to date has been used in conjunction with bitcoin – holds promise in establishing a new trusted framework for existing business models and securely scaling the Internet of Things. Blockchain technology puts all the control of personal information directly in each owner's hands, and then uses a digital ledger to privately share only the needed details for a transaction to only the parties who need this data.

But while blockchain technology has the big potential to transform business operating models in the long term, what are the near-term challenges for engineering organizations who want to adopt the technology? How might it disrupt traditional design flows and methodologies?

PANELISTS:

James Gambale - *Lomasoft Corp., San Diego, CA*
George Alexy - *BaySand, Inc., San Jose, CA*

CORE CHOICES: HOW TO NAVIGATE THE BRAVE NEW WORLD OF IP

Date: Tuesday, June 26 || Time: 3:00 - 3:45pm || Room: DAC Pavilion - Booth 2161
Keywords: Emerging Architectures & Technologies || Topic Area: IP, Design

MODERATOR:

Junko Yoshida - *EE Times, San Francisco, CA*

ORGANIZER:

Michelle Clancy - *Cayenne Communication, Sunnyvale, CA*

Four decades into the evolution of IP core design, the landscape continues to evolve. The demands of SoC designs—and ultimately end systems — have always been fertile ground for innovation and new approaches. This in part has spurred the rise of the free and open RISC-V instruction set architecture (ISA) movement. Yet long-time industry players such as Arm, Synopsys, Cadence, Ceva and MIPS are not standing still, and continue to rapidly evolve their technology and business. New technologies, alliances, acquisitions and approaches give engineers the broadest choice ever, but with this flexibility come new challenges. This panel will offer stimulating insights that will help you navigate this evolving IP world.

PANELISTS:

Rick O'Connor - *RISC-V Foundation, Berkeley, CA*
John Ronco - *Arm, Ltd., Cambridge, United Kingdom*
Majid Bemanian - *MIPS Technologies, Inc., Santa Clara, CA*
Markus Levy - *NXP Semiconductors, Austin, TX*

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TEARDOWN: OTII ARC ENERGY OPTIMIZATION SYSTEM

Date: Tuesday, June 26 || Time: 4:30 - 5:00pm || Room: DAC Pavilion - Booth 2161
Keywords: Emerging Architectures & Technologies || Topic Area: Machine Learning/AI

ORGANIZER:

Michelle Clancy - *Cayenne Communication, Sunnyvale, CA*

Power consumption in battery-driven IoT devices is critical, so any device that helps quickly zero in on a design's power consumption in the prototype and layout stage is more than welcome. One such device is the Otii Arc from Qoitech. Combining both power supply and energy consumption monitoring in one device, the Otii Arc connects to the device under test (DUT) using 4-mm connectors and sends all related data to a PC over a USB cable.

To see how it does this, DAC has partnered with Electronic Design and ClariTek to take a look inside the Otii Arc. In talking with Qoitech, we're even more excited about this, because it's very much in "the raw." Think: Wires! The next iteration of the system will be more refined, Qoitech tells us. That's good, but at DAC we'll see first-hand the raw version, and talk with Qoitech about how it plans to refine the design.

What's more, attendees at the Teardown Event will get their names put in a hat to win a brand new Otii Arc to take home! Come join this exciting, insightful, Teardown Event to see where the state-of-the-art in IoT device energy monitoring and optimization.

SPEAKER:

Patrick Mannion - *ClariTek, LLC, Commack, NY*

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HOW DEEP LEARNING STARTUPS ARE DRIVING THE SILICON WORLD

Date: Wednesday, June 27 || Time: 10:30 - 11:00am || Room: DAC Pavilion - Booth 2161
Keywords: Emerging Architectures & Technologies || Topic Area: Machine Learning/AI, Design

Deep learning is all the rage, and this enthusiasm is most evident in the explosion of startup companies leveraging this revolutionary model of computation. Training and inference of deep neural networks are fundamentally intensive in both computation and memory demands, so the spread of deep learning may have a profound impact on the silicon world. In this talk, I analyze the state of the deep learning startup universe, with particular attention to three distinct dimensions of the change - use of deep learning in mainstream EDA, the potential for EDA-like tool innovations in neural network design, and most especially, the design of new silicon platforms for deep learning. The on-going renaissance in chip startups reveals important trends in computation structures, memory system, parallelism, software environments, business models and venture funding. I conclude with a roundup of the startups particularly worth watching and the emerging formulas for success.

SPEAKER:

Chris Rowen - *Babblabs, Inc, San Jose, CA*

STRAIGHT TALK WITH NAVEED SHERWANI, CEO OF SIFIVE

Date: Wednesday, June 27 || Time: 11:30am - 12:15pm || Room: DAC Pavilion - Booth 2161
Event Type: DAC Pavilion || Keywords: Emerging Architectures & Technologies
Topic Area: EDA, Machine Learning/AI

MODERATOR:

Ed Sperling - *SemiEngineering Magazine, San Jose, CA*

SiFive's CEO sits down with Semiconductor Engineering's Ed Sperling to discuss what's changing in chip architectures, including where open-source hardware fits in, who's using it and why, and how this plays with other chip architectures. What are the advantages and disadvantages of an architecture that can be modified by vendors?simulated, and that it's secure, and how do we manage both the behavior and the reliability of these systems as they increasingly interact with other systems.

SPEAKER:

Naveed Sherwani - *SiFive, Inc., San Mateo, CA*

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HACK ME IF YOU CAN: HANDS-ON IOT HACKING

Date: Wednesday, June 27 || Time: 1:30 - 5:00pm || Room: DAC Pavilion - Booth 2161
Keywords: Test & Verification, Contests, Any || Topic Area: Security/Privacy, IoT

ORGANIZERS:

Michail Maniatakos - *New York Univ., Abu Dhabi, United Arab Emirates*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

System designers often overlook security vulnerabilities in their designs. These vulnerabilities are pervasive and are more pronounced in embedded systems. Embedded systems are more attractive targets of hacking because they are either widely prevalent and low-cost, and thus not necessarily provide high-end security features while handling sensitive information, or they are legacy devices built and installed decades ago without concern about cybersecurity.

In this session, experts will demonstrate real-world hacks and how they can exploit vulnerabilities in widely-used embedded devices, ranging from fitness trackers to devices used in critical infrastructure. The objective is to create awareness among the attendees on security research and security-enabled system design. They will provide hands-on training, such that the attendees can perform security analyses on similar embedded devices and improve their security.

Schedule of Events

1:30pm: Presentation

2:00pm: Hacking Session 1: Fitness Trackers

3:00pm: Hacking Session 2: PLCs

4:00pm: Hacking Session 3: Switches/Routers and Laser Printers

SPEAKERS:

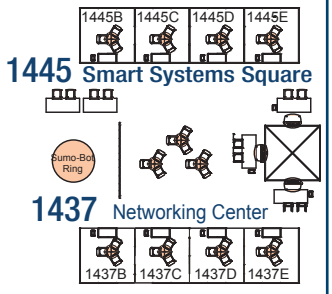
Michail Maniatakos - *New York Univ., Abu Dhabi, United Arab Emirates*
Anastasis Keliris - *New York Univ., Abu Dhabi, United Arab Emirates*
Ang Cui - *Red Balloon Security, New York, NY*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Markus Miettinen - *Technische Univ. Darmstadt, Germany*
Richard Mitev - *Technische Univ. Darmstadt, Germany*

SMART SYSTEMS SQUARE

Detect - Decide - Do

Orange highlight denotes First Time Exhibitors

Corigine, Inc.	1445B
Xilinx	1445C
AGGIOS, Inc.	1445D
Logic Fruit Technologies	1445E
NEC Corporation	1437B, 1437C
NVIDIA	1437D
Westghats Technologies	1437E



W1

WORKSHOP 1: THE THIRD INTERNATIONAL WORKSHOP ON DESIGN AUTOMATION FOR CYBER-PHYSICAL SYSTEMS (DACPS)

Time: 8:00am - 5:00pm || Room: 3022 || Event Type: Workshop || Keywords: Architecture & System Design, Emerging Architectures & Technologies || Topic Area: Design, IoT

ORGANIZERS:

Qi Zhu - *Northwestern Univ., Evanston, IL*
Mohammad Al Faruque - *Univ. of California, Irvine, CA*
Chung-Wei Lin - *Toyota InfoTechnology Center, Mountain View, CA*
Shiyan Hu - *Michigan Technological Univ., Houghton, MI*
Yier Jin - *Univ. of Florida, Gainesville, FL*
Bei Yu - *Chinese Univ. of Hong Kong, China*
Huafeng Yu - *Boeing, Huntsville, AL*

Cyber-Physical Systems (CPS) are characterized by the strong interactions between cyber and physical components. CPS system examples include automotive and transportation systems, avionics systems, smart home, building and community, smart battery and energy systems, robotic systems, cyber-physical biochip, wearable devices, and so on. Due to the deeply complex intertwining among different components, CPS designs pose fundamental challenges in multiple aspects such as safety, performance, security, reliability, fault tolerance, extensibility, and energy consumption. Developing innovative design automation techniques, algorithms and tools is imperative to address the unique challenges in CPS design and operation, such as the fast increase of system scale and complexity, the close interactions with dynamic physical environment and human activities, the significant uncertainties in sensor readings, the employment of distributed architectural platforms, and the tight resource and timing constraints. This workshop will present the state-of-the-art research results on the topic of design automation for CPS/IoT systems, introduce practical challenges and promising solutions in various industry sectors, and stimulate CAD researchers to participate in the interdisciplinary CPS/IoT research. In addition to the regular submissions, this workshop will also seek invited submissions/talks from high-profile experts in both academia and industry.

SPEAKERS:

Edward Lee - *Univ. of California, Berkeley, CA*
Natarajan Shankar - *SRI International, Menlo Park, CA*
Alessandro Pinto - *United Technologies Research Center, Berkeley, CA*
Sandip Ray - *Univ. of Florida, Gainesville, FL*
Wenchao Li - *Boston Univ., Boston, MA*
Chung-Wei Lin - *Toyota InfoTechnology Center, Mountain View, CA*
Takashi Ichimasa - *Mentor, A Siemens Business, Fremont, CA*

W2

WORKSHOP 2: PHYSICAL ATTACKS AND INSPECTION ON ELECTRONICS (PAINE)

Time: 8:00am - 5:00pm || Room: 3020 || Event Type: Workshop || Keywords: Any Topic Area: Security/Privacy, IoT

Physical attacks on electronics have grown significantly recently and is becoming a major threat to the chip designers, original equipment manufacturers as well as end users. The complex long life of the emergent internet of things (IoT) devices coupled with their diverse applications are making them increasingly vulnerable to various forms of physical attacks. A large number of companies and start-ups are now working in this area across the globe and offer training and service to the public. As importantly, the number of the programs introduced by US government has increased hugely to analyze and find a solution for this problem. High-end failure analysis tools, which used to be very expensive and accessible to only big organizations are now available for a cheaper price. Private parties can now buy such tools and rent them to the public with a very low rate, which makes these attacks ever more viable. In addition to physical attacks, physical inspection of electronics as well as physical fingerprinting based on analog parameters are rapidly becoming a tool for unique countermeasures against various attack modalities.

This workshop will be the first step to start the conversation on such topics in US for the first time and will include all forms of physical attacks and countermeasures, including, but not limited to, side-channel attacks, reverse engineering, physical tampering, micro/nano probing, and physical access at chip, PCB and system level.

W3

WORKSHOP 3: SUNDAY SUMO ROBOT CLASS

Time: 8:00am - 12:00pm || Room: 3016 || Event Type: Workshop
Keywords: Emerging Architectures & Technologies

This hands-on class gets the participants up to speed and enables them to get their robots programmed so they can compete in the Sumo competition. Participants receive a pre-built and assembled Zumo 32U4 robot from Pololu which are used in the Sumo battle event on Wednesday at the conference. Participants need to bring their own Notebook (Requirements: see https://www.arduino.cc/en/Main/Software)

Introduction to Mini Sumo Robotics and competition rules. Hands-on lab for how to build and program a Mini Sumo Robot. How to drive the DC motors with quadrature encoders. How to use the IR reflectance sensor to detect the Dohyo border. How to use sensors to detect the opponent. How to optimize a Mini Sumo Robot for the competition: calibration and best usage of sensors, battle strategies, tips & tricks for competition.

Agenda:

- Start: handing out the robots, cables, batteries and charger
- Sumo: rules of the competition
- Overview: hardware overview, components of the robot: power, sensors, actuators and microcontroller, expansion areas
- First Steps: exploring the LCD menu, using LEDs, buzzer, IR sensor, encoder and motors
- IDE: installation of the Arduino IDE, serial drivers and libraries
- Bootloader and loading programs
- Hands-On: The first program blinking a LED on the robot
- Hands-On: LEDs, buttons and buzzer
- Hands-On: LCD
- Hands-On: Line Sensors and Border Detect
- Hands-On: Motors and Position Encoders
- Hands-On: Opponent Detection
- Hands-On: Inertial Sensor and Collision Detection
- Sumo battles Tips & Tricks

Sumo robot competition at DAC:
The Dohyo ring will be set up on the DAC exhibition floor in the Smart Systems Square booth # 1437 for pre-competition practice. All Sumo tutorial attendees are encouraged to practice and compete.

Pre-competition practice will be held:
10:00am – 5:00 pm on Monday, June 25th
10:00am – 12:00 pm on Tuesday, June 26th

The final competition will be held 6:00pm at the DAC Tuesday night reception.

SPEAKER:

Erich Styger - *University of Lucerne, Switzerland*

W4

WORKSHOP 4: DAC WORKSHOP ON MACHINE LEARNING IN DESIGN AUTOMATION (MALENDA)

Time: 8:45am - 5:00pm || Room: 3024 || Event Type: Workshop
Keywords: Architecture & System Design, Emerging Architectures & Technologies, Logic & High-Level Synthesis || Topic Area: Machine Learning/AI, EDA

ORGANIZER:

Rasit Topaloglu - *IBM Corp., Hopewell Junction, NY*
Andrew Kahng - *Univ. of California, San Diego, La Jolla, CA*

Machine learning is going full steam across several industries. Due to massive processing power and architectures that are honed to train large datasets, applications once thought to be infeasible are targeted now by machine learning algorithms. EDA has started to look into this area and utilize some of these ideas, at least on paper.

There is a nice contrast though. EDA is a domain that is shaped with heuristics and tens of other algorithms and mathematical methodologies. Can Machine Learning claim its own territory for certain EDA applications? Can existing algorithms be sped up by using machine learning specific architectures instead?

We think that by bringing in both proponents of machine learning and traditional incumbents together, we can discuss what could be some of the best research and development directions for EDA in this area. We also plan to bring in people from external machine learning communities to get their view on the applicability to problems in our domains. We plan to build on these dynamics and educate the attendees on machine learning in general as well. The workshop consists of invited talks, panels, tutorials, and posters.

SPEAKERS:

Manish Pandey - *Synopsys, Inc., Mountain View, CA*
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*
Duane Boning - *Massachusetts Institute of Technology, Cambridge, MA*
Norman Chang - *ANSYS, Inc., San Jose, CA*
Soha Hassoun - *Tufts Univ., Medford, MA*
Andrew Kahng - *Univ. of California, San Diego, La Jolla, CA*
David Pan - *Univ. of Texas at Austin, TX*
Jinjun Xiong - *IBM Corp., Yorktown Heights, NY*

PANELISTS:

Rajeev Jain - *Qualcomm, Inc., San Diego, CA*
Paul Franzon - *North Carolina State Univ., Raleigh, NC*
Brucek Khailany - *NVIDIA Corp., Santa Clara, CA*

W5

WORKSHOP 5: RISC-V ECOSYSTEM - RESHAPING THE CPU LANDSCAPE

Time: 1:00 - 4:00pm || Room: 3018 || Event Type: Workshop || Keywords: Architecture & System Design, Emerging Architectures & Technologies || Topic Area: Design

DAC Workshop: RISC-V Ecosystem - Reshaping the CPU Landscape
This talk will detail how the free and open RISC-V instruction set architecture (ISA) is creating a paradigm shift in industry, reinvigorating semiconductor design and reshaping traditional business models.

RISC-V ISA and Foundation Overview
Rick O'Connor - *RISC-V Foundation, Berkeley, CA*

This session will present RISC-V, a free and open ISA. With broad industry adoption, RISC-V is finding its way into applications ranging from IoT to high end servers and supercomputing. This session provides an ISA introduction and a RISC-V Foundation overview.

RISC-V - A Diversity of Core and Accelerator Choices
Markus Levy - *NXP Semiconductors, El Dorado Hills, CA*

This talk will present some of the notable aspects that make RISC-V attractive: formal support for different instruction subsets, the range of OS support (bare metal to hypervisor) and extensibility for custom instructions. The session will review a few of the different RISC-V cores available and provide design considerations of a microcontroller-based core.

RISC-V OS Landscape - Palmer Dabbelt - *SiFive, Berkeley, CA*

This talk will give an overview of the RISC-V operating systems landscape. The session will cover operating systems such as Zephyr and other RTOS offerings that target IoT/microcontroller applications. Attendees will also learn about embedded Linux distributions such as Yocto Linux as well as desktop/server operating systems such as Fedora, Debian, and FreeBSD.

Designing a custom RISC-V core using Chisel - Alex Badicioiu - *NXP Semiconductors, El Dorado Hills, CA*

In this session, we will show a hands on demo of the steps required to create custom instruction extensions for RISC-V using available open source tools.

DESIGN AUTOMATION SUMMER SCHOOL

Date: Sunday, June 24 || Time: 7:30am - 6:00pm || Room: 3003
Event Type: Additional Meeting || Keywords: Architecture & System Design
Topic Area: EDA, General

ORGANIZERS:
Jier Jin - *Univ. of Central Florida, Orlando, FL*
Muhammad Shafique - *Technische Univ. Wien, Vienna, Austria*
Jayita Das - *Intel Corp., Hillsboro, OR*

The Design Automation Summer School (DASS) is a one-day intensive course on research and development in design automation (DA). Each topic in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments, and indicate remaining challenges. This program is intended to introduce and outline emerging challenges, and to foster creative thinking in the next generation of EDA engineers.

The 2018 SIGDA Design Automation Summer School is co-hosted by A. Richard Newton Young Fellowship Program at DAC. All the students receiving the fellowship (excluding the mentors) are required to attend the DASS event.

For additional details go to: http://www.sigda.org/dass

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A. RICHARD NEWTON YOUNG FELLOW PROGRAM WELCOME BREAKFAST & ORIENTATION

Date: Sunday, June 24 || Time: 7:30am - 9:00am || Room: 3003
Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Welcome Breakfast and Orientation
Sunday, June 24
7:30 - 9:00am
Room: 3003

Poster Presentation (Colocated with the Ph.D. Forum)
Tuesday, June 26
7:00 - 9:00pm
Level 3 Lobby

Closing Session and Award Ceremony
Thursday, June 28
6:00 - 6:45pm
Room: 3003

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ACM/IEEE EARLY CAREER WORKSHOP AT DAC

Sunday, June 24 || Time: 8:30am - 6:00pm || Room: 3014
Event Type: Additional Meeting || Keywords: Any || Topic Area: Design, EDA

ORGANIZERS:
Avrial Shrivastava - *Arizona State Univ., Tempe, AZ*
Andreas Gerstlauer - *Univ. of Texas at Austin, TX*
Shishpal S. Rawat - *IEEE Council on Electronic Design Automation, Folsom, CA*
Sherie Taylor - *Intel Corp., Chandler, AZ*

This workshop is for young and mid-career faculty and professionals in the fields related to electronic design automation (EDA). The workshop will start in the morning with an interactive session borrowing techniques from IMPROV to help you improve your soft skills (interpersonal, communication etc.) with others. This is followed by presentations and panel discussions by professionals discussing diverse topics such as navigating the various challenges to better succeed and thrive in your academic or industry job, getting your projects funded and climbing academic and technical ladders, as well as improved cooperation between industry and academia research and development. In addition, the workshop will provide rich opportunities to closely interact and network with some of the established academicians, professionals, and funding officers in EDA related fields.

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OPENING SESSION & AWARDS PRESENTATION

Time: 9:00am - 9:20am || Room: 3008

Join us as we set the stage for the 55th DAC! DAC's Executive Committee will highlight the conference's events, and the award presentations will recognize success and excellence for individuals in the field of design automation of electronic systems.

2017 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO ELECTRONIC SYSTEM DESIGN

Dr. Rob A. Rutenbar, Senior Vice Chancellor for Research at the University of Pittsburgh

Dr. Rutenbar is being honored for his contributions to analog design automation and impact on EDA education. As an academic, he developed a wide range of fundamental models, algorithms and tools for analog IC designs. As an entrepreneur, he co-founded Neolinear, one of the most successful analog tool companies, to bring his research efforts to a larger design community. (Neolinear was acquired by Cadence in 2001.)

A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Dr. Hans Eisenmann, PDF Solutions GmbH, Formerly Technische Universität München; The Late Frank M. Johannes, Formerly Technische Universität München.

Sponsored by the IEEE Council on Electronic Design Automation and the ACM Special Interest Group on Design Automation. For seminal contributions to VLSI placement impacting academia and industrial practices.

Hans Eisenmann and Frank M. Johannes, "Generic Global Placement and Floorplanning" Proc. of the 35th Design Automation Conference, pp. 269 – 274, June 1998.

2018 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

Anne Cirkel, Senior Director for Technology Marketing at Mentor, a Siemens Business

This annual award, named for Marie R. Pistilli, the former organizer of DAC, recognizes individuals who have visibly helped advance women in Electronic Design.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIP FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

Myles Cherebin

The objective of the P.O. Pistilli Undergraduate Scholarship for Advancement in Computer Science and Engineering is to increase the pool of professionals in Electrical and Computer Engineering and Computer Science from under-represented groups (female, African-American, Hispanic, Native American, and disabled students). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. DAC funds a $4,000 scholarship, renewable up to five years, to graduating high school seniors who have a 3.00 GPA or better
(on a 4.00 scale).

DAC UNDER-40 INNOVATORS AWARD

The Under-40 Innovators Award is sponsored by Association for Computing Machinery (ACM), the Electronic Systems Design Alliance (ESDA), and the Institute of Electrical and Electronics Engineers (IEEE). The award will recognize the top five young innovators (nominees should be 40 years or younger in age as of June 1, 2018) who are movers and shakers in the field of design and automation of electronics.

SYSTEM DESIGN CONTEST WINNERS

HACK@DAC WINNERS

KEYNOTE: LIVING PRODUCTS: BUILDING CONNECTED DEVICES THAT LEARN AND EVOLVE

SARAH COOPER – *GM of IoT Solutions, Amazon Web Services, Inc., Mountain View, CA*

Time: 9:20am - 10:00am || Room: 3008 || Keywords: Architecture & System Design, Emerging Architectures & Technologies, Reconfigurable Systems Topic Area: IoT, Machine Learning/AI

It took powerful hardware platforms to enable the ecosystem that turned mobile phones from communication devices to personal assistants, shopping portals, gaming consoles, and so much more. Connected products need a similar transformation from individual actors performing essentially the same function just better to an interconnected backdrop of data driving dynamic device collaboration proactively building consumer experiences, i.e. ambient intelligence. Are recent advancements in embedded AI, security, remote management and end-to-end tools enough to drive ambient intelligence or do we need more?

Biography: Dr. Sarah Cooper is AWS's GM of IoT Analytics and Applications. With 15yrs experience building IoT devices and platforms, Sarah serves as vice chairwoman of the Internet of Things Community, a 20,000 member organization dedicated to education and information sharing amongst the IoT practitioner community. Formerly, M2Mi's Chief Operating Officer, Sarah was named an IS 50 Most Empowering Women in Business, recognized Top 100 Wireless Technology Expert by Wireless World, a top 20 IoT Influencer by Inc. magazine and a National Academy of Engineers Frontiers of Engineering Awardee. Sarah founded and sold TE-Bio, an IoT device company, NaturalNano, an advanced nanomaterials company and conducted fundamental research at NASA and DoE. She holds a PhD in Physics from the University of Sydney and patents in advanced materials and devices.

DT1 DESIGNER TRACK: EMBEDDED SYSTEM SOFTWARE, MACHINE LEARNING AND SECURITY

Time: 10:30am - 12:00pm || Room: 2012 || Event Type: Designer Track Reviewed
Keywords: Embedded System Software || Topic Area: ESS, IoT

CHAIR:
Natarajan Ekambaram - *NXP Semiconductors, Austin, TX*

This session explores state-of-the art embedded system software, machine learning, deep learning neural networks and security architectures.

1.1 System Performance and Optimizations for Deep Learning
Mihai Caraman - *NXP Semiconductors, Bucharest, Romania*

1.2 INSPEX: Integrated Portable Multi-sensor Obstacle Detection Device Application to Navigation for Visually Impaired People
Olivier Debicki, Nicolas Mareau, Laurent Ouvry, Julie Foucault - *CEA, Grenoble, France*
Suzanne Lesecq - *CEA-LETI Minatec, Grenoble, France*
Gabriela Dudnik, Marc Correvon - *Centre Suisse d'Electronique et Microtechnique SA, Neuchatel, Switzerland*

1.3 Energy-efficient Voice Recognition on Constrained Devices
Chris Shore - *Arm Ltd., Cambridge, United Kingdom*

1.4 Layered Security: Flexible Application of Embedded RoT & Camouflaged Designs
Michael Y. Chen - *Mentor, A Siemens Business, Wilsonville, OR*

1.5 Extended CPS Simulation for EMC Compliance of Automotive IC Chip Developments
Akihiro Tsukioka, Makoto Nagata - *Kobe Univ., Kobe, Japan*
Takao Egami, Rieko Akimoto, Kenji Niinomi, Takeshi Yuhara, Sachio Hayashi - *Toshiba Electronic Devices & Storage Corp., Kawasaki, Japan*
Karthik Srinivasan, Ying-Shiun Li, Norman Chang - *ANSYS, Inc., San Jose, CA*

1.6 Machine Learning Inference on Arm Client and Embedded Devices
Jason Andrews - *Arm Ltd., Minneapolis, MN*
Odin, Luen-Ming, Shen - *Arm Ltd., Taipei City, Taiwan*

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DT2 DESIGNER TRACK: VERIFICATION METRICS FROM CORES TO SYSTEMS: ARE CONVENTIONAL METRICS RUNNING OUT OF STEAM?

Time: 10:30am - 12:00pm || Room: 2010 || Event Type: Designer Track Panel
Keywords: Test & Verification, Architecture & System Design || Topic Area: Design, IP

MODERATOR:
Ann Steffora Mutschler - *Semiconductor Engineering, San Jose, CA*

ORGANIZER:
Hemendra Talesara - *Advanced Micro Devices, Inc., Austin, TX*

As designs complexity has multiplied, verification complexity has exploded. Verification has become an art of applying many unique methodology for each of the different classes of sub-design within a design. How do we measure quality? How do we measure success? Some of the key metrics such as coverage produces more data than we could have imagined. Are we on the right track? How about at the System level? Do these metrics even apply? In this invited session Industry leaders will debate different verification metrics. What works for them and what does not and where do we go from here?

PANELISTS:
Alan Hunter - *Arm Ltd., Austin, TX*
Maruthy Vedam - *Intel Corp., Santa Clara, CA*
Anshuman Nadkarni - *NVIDIA Corp., Santa Clara, CA*
Farhan Rahman - *Advanced Micro Devices, Inc., Austin, TX*

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IP3

IP TRACK: HARDWARE IP FOR DEEP LEARNING

Time: 10:30am - 12:00pm || Room: 2008 || Event Type: IP Track Invited
Keywords: Emerging Architectures & Technologies, Architecture & System Design
Topic Area: IP, Machine Learning/AI

CHAIR & ORGANIZER:

Paul Stravers - *Synopsys, Inc., Eindhoven, The Netherlands*

The market for deep learning applications is predicted to grow at a 65% annual rate in the next 5 years. The growth is fueled by innovative hardware architectures that bring artificial intelligence to devices at the edge of the internet and at its core. Examples include voice assistants, face-based authentication, big data analytics and self-driving vehicles. Established companies as well as numerous semiconductor startups are introducing a diverse range of deep learning IP, and no winner has been declared yet. In this invited session players from industry and academics present their architecture, with programming examples and applications.

3.1 Understanding the Limitations of Existing Energy-efficient Design Approaches for Deep Neural Networks
Vivienne Sze - *Massachusetts Institute of Technology, Cambridge, MA*

3.2 Achieving High MAC Utilization for Efficient Implementation of Deep Learning Algorithms on Embedded Hardware
David Heine, Himanshu Sanghavi - *Cadence Design Systems, Inc., San Jose, CA*

3.3 Cambricon's Deep Learning Processor
Shuai Chen - *Cambricon Technologies Corp., Ltd., Beijing, China*

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IEEE CEDA AUTHOR EDUCATION TALK: ACADEMIC PUBLISHING: MANGLED MEANS AND TATTERED ENDS IN FASCINATING TIMES

Time: 10:30 - 11:30am || Room: 3014 || Event Type: Additional Meeting
Keywords: Any || Topic Area: EDA

ORGANIZERS:

Gi-Joon Nam - *IBM Research, Yorktown Heights, NY*
Miguel Silveira - *INESC-ID/IST - TU Lisbon, Lisboa, Portugal*

Sachin Sapatnekar formulated the Promising Author Problem and cast into an optimization problem in a true blue-blood EDA researcher's fashion. This talk looks at publishing from the other end of the publication pipeline, the Punished Publisher Problem as the existential absurdity of the publication enterprise. There may be lessons in this talk, though lunch is likely to have a higher value.

SPEAKER:

Rajesh Gupta - *Univ. of California, San Diego, La Jolla, CA*

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SKY TALK: AUTOMATING INTELLIGENCE: MACHINE LEARNING AND THE FUTURE OF MANUFACTURING

Time: 1:00 - 1:25pm || Room: DAC Pavilion - Booth 2161 || Event Type: SKY Talk
Keywords: Emerging Architectures & Technologies
Topic Area: Machine Learning/AI

ORGANIZER:

McKenzie Ross - *Worldwide Women in Electronic Design (WWED) & OneSpin Solutions GmbH, Campbell, CA*

There are a lot of buzzwords floating around the manufacturing world these days: IoT, AI, machine learning, deep learning, Industry 4.0 … all these words sound impressive, but what's actually going on? Anna-Katrina Shedletsky dives into real-world examples of how automation and greater access to manufacturing data is enabling the rise of manufacturing intelligence. She covers a brief background on factory automation, discusses what buzzwords actually mean for the industry, and presents case studies on how machine learning algorithms are already aiding anomaly detection on assembly lines. To wrap up, Anna looks to the future of automation, explaining from personal experience how it has the potential to help companies from a broad range of sectors to dramatically reduce build delays and costly product recalls.

SPEAKERS:

Anna-Katrina Shedletsky - *Instrumental, Inc., Los Altos, CA*

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DT4 DESIGNER TRACK: WITH POWER COMES RESPONSIBILITY

Time: 1:30 - 3:00pm || Room: 2012 || Event Type: Designer Track Reviewed
Keywords: Low-Power & Reliability || Topic Area: Design, EDA

CHAIR:
Badhri Uppiliappan - *Analog Devices, Inc., Boston, MA*

In this session, we explore managing power and its consequences. We start off with circuit techniques to reduce power, moving through low power design implementation and analytical methods to build robust power delivery networks. We finish the session by peering into the collaboration of "Man Machine Methods" to help ease predictions.

4.1 Ultra Low Power True Single Phase Master Slave Flip-flop Architectures - A Case for its Usage in Energy-efficient Designs
Deepon Saha, Arun Iyer - *Advanced Micro Devices, Inc., Bangalore, India*

4.2 Power Management Implementation Methodology for Ultra-low-power Designs
Gaurav K. Varshney, Venkatraman Ramakrishnan, Aswani K. Golla, Sangram S. Thopte - *Texas Instruments India Pvt. Ltd., Bangalore, India*

4.3 High Coverage Multi-variable Build Quality Metrics in Power Integrity Signoff
Kritika Garg, Emmanuel Chao, Santosh Santosh - *NVIDIA Corp., Santa Clara, CA*
Scott Johnson, Tom Taylor - *ANSYS, Inc., San Jose, CA*
Sooyong Kim - *ANSYS, Inc., Palo Alto, CA*

4.4 A Novel Multi-cycle Vectorless Dynamic IR Signoff Flow to Capture Hotspots and Achieve near 100% Coverage
Huajun Wen, Hugh Mair, Hsinchen Chen, Rolf Lagerquist - *MediaTek, Inc., Austin, TX*
Chee-kong Ung, Chin-chuan Lim - *MediaTek, Inc., Hsinchu City, Taiwan*
Wailing Cheng - *MediaTek, Singapore Pte. Ltd., Singapore*
Siddalingesh Tenginakai, Sankar Ramachandran - *ANSYS, Inc., Bangalore, India*

4.5 Efficiently Capturing Heterogeneity in Self Heating Analysis of Next Generation High-performance Microprocessor Designs
Arun Joseph - *IBM Systems and Technology Group, Bangalore, India*
Arya Madhusoodhanan - *IBM Systems Group, Bangalore, India*
Spandana Rachamalla - *IBM Corp., Bangalore, India*
Nagu Dhanwada - *IBM Corp., Poughkeepsie, NY*
Shashidhar Reddy - *IBM Systems Group, Bangalore, India*

4.6 AI/ML Application on IR Drop Prediction
Dean Sheng-Chih Huang, Howard Po-Hao Chen - *MediaTek, Inc., Hsinchu, Taiwan*
Yen-Chun Fang, Heng-Yi Lin, James Chien-Mo Li - *National Taiwan Univ., Taipei, Taiwan*
Eric Jia-Wei Fang, Fwu-Juh Huang - *MediaTek, Inc., Hsinchu, Taiwan*
Dajen Huan - *MediaTek, Inc., San Jose, CA*

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DT5 DESIGNER TRACK: INDUSTRIAL-STRENGTH ACCELERATORS FOR MACHINE LEARNING AND ARTIFICIAL INTELLIGENCE

Time: 1:30 - 3:00pm || Room: 2010 || Event Type: Designer Track Invited
Keywords: Architecture & System Design, Emerging Architectures & Technologies
Topic Area: Machine Learning/AI, Design

CHAIRS & ORGANIZERS:
Gert Cauwenberghs - *Univ. of California, San Diego, CA*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

The recent surge of interest and commercial development in deep learning and artificial intelligence is impacting all areas of science and engineering where massive data can be harnessed to make autonomous decisions in real-time, ranging from consumer choice analytics and medical diagnosis to driverless cars. The key enabling factor that is fueling this revolution in pervasive computational intelligence is the seemingly limitless availability of data and computational power. New architectural advances in alternative non-von Neumann computing are needed to address design challenges faced in extending the relentless pace of exponential growth to sustain continued advances. This session highlights such new and emerging developments in large-scale accelerator hardware and software for deep learning and adaptive computational intelligence, including testimony by three companies in the IT marketplace: Intel, Facebook, and DeePhi.

5.1 The Loihi Research Chip: A Step Towards Scalable and Efficient On-Chip Learning
Mike Davies - *Intel Corp., Hillsboro, OR*

5.2 Systematic Solution for Edge Deep Learning: From Accelerator to Software Eco-System
Song Yao - *DeePhi Tech., Beijing, China*

5.3 Benchmark Data Driven Co-design for Neural Network Applications
Fei Sun - *Facebook, San Jose, CA*

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IP6 IP TRACK: MINIMIZING IC POWER CONSUMPTION WITH PPA OPTIMIZED IPS

Time: 1:30 - 3:00pm || Room: 2008 || Event Type: IP Track Panel || Keywords: Low-Power & Reliability, Architecture & System Design, Analog & Mixed-signal Design Topic Area: IP, Design

MODERATOR:

John Blyler - *JB Systems & Portland State Univ., Portland, OR*

ORGANIZER:

Farzad Zarrinfar - *Mentor, A Siemens Business, Fremont, CA*

Low power techniques are essential for introducing differentiated products to gain/keep market share. Applications like Artificial Intelligence, IOT, Deep Learning, Automotive, Virtual Reality, and wearable computing are transforming semiconductor industry and driving for low power IP strategies. In this panel, implementation techniques and tradeoffs for designing ultra Low-power SIP (Semiconductor IP), SOCs, ASSPs, and ASICs will be presented. These techniques are critical for battery-powered devices as well as reduction of packaging cost. IP suppliers and EDA vendors now offer low-power IPs as well as optimization tools. Topics such as FinFet and FDSOI devices will be compared with planar CMOS. Designers also apply advanced techniques by reduced voltage or Dynamic Voltage & Frequency Scaling (DVFS), power shutdown, dual-rail memory IPs, shutoff modes, and retention logic with resource sharing. Advanced low-power designs could have over 30 different power modes and power domains will be discussed.

PANELISTS:

Lluis Paris - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*
Aditya Mukherjee - *Microsoft Corporation, Mountain View, CA*
Sarvesh Shrivastava - *TDK Corp., San Jose, CA*
Tuomas Hollman - *Minima Processor, Fremont, CA*
Frederic Renoux - *Dolphin Integration, Grenoble, France*
Saurabh Shrimal - *Mentor, A Siemens Business, Noida, India*

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DT7 DESIGNER TRACK: FINDING PATTERNS AND INFERENCES

Time: 3:30 - 5:00pm || Room: 2012 || Event Type: Designer Track Reviewed Keywords: Physical Design & DFM, Low-Power & Reliability || Topic Area: Design, EDA

CHAIR:

Sabya Das - *Xilinx Inc., San Jose, CA*

This session explores robust and efficient failure analysis and fix-up techniques to address issues from manufacturability to ESD protection. The session starts with the use of pattern matching and classification techniques for DFM and memory array verification. We then see how machine learning can be used to aid these computationally intensive steps. This is followed by a fast method to identify CDM failures. We end this session with a view of constructing large-scale graph databases for efficient post-design analyses.

7.1 Fast Foundry-certified In-design and Signoff Lithography Physical Analysis Based on OPC Production Model, Recipe and Engine
Ahmed Elsemary, Mohamed Ismail, Janam T. Bakshi, Mohamed Omnia - *GLOBALFOUNDRIES, Santa Clara, CA*
Paul Schroeder - *GLOBALFOUNDRIES, San Jose, CA*
Sriram Madhavan - *GLOBALFOUNDRIES, Santa Clara, CA*
Michel Côté, Ya-Chieh Lai, Jac Condella, David Lay, Philippe Hurat - *Cadence Design Systems, Inc., San Jose, CA*
Vincent Arnoux, Stanislas Baron, Ahmad Elsaid, Ronald Goossens, Ahmed Khalil, Pengcheng Li, Mohamed M.Ali Mohamed, Hesham Omar, Cyrus Tabery, Jun Ye, Daniel W. Yergeau, Xuefeng Zeng - *ASML, San Jose, CA*

7.2 Memory Array Verification - A Pattern-based Approach
Baby Praveen Kollery, Venkatasubraminan Krishnamoorthy - *Arm Ltd., Bangalore, India*
Gurpreet S. Lamba - *Mentor, A Siemens Business & Mentor Graphics (India) Pvt. Ltd., Bangalore, India*
Nermeen Hossam - *Mentor, A Siemens Business, Cairo, Egypt*

7.3 An Automated Methodology for Optimizing Lithography Weak-Points using Partial Pattern Matching Technique
Shobhit Malik - *GLOBALFOUNDRIES, Santa Clara, CA*
Vikas Tripathi, Yongfu Li, I-Lun Tseng, ZhaoChuan Lee, Yoong Seang Ong, Valerio Perez - *GLOBALFOUNDRIES, Singapore*

7.4 In-design Layout Hotspot Prediction using Machine Learning with Automated Fixing
Jaehwan Kim - *Samsung Electronics Co., Ltd. & Samsung Semiconductor, Inc., Gyunggi-do, Republic of Korea*
Piyush Pathak - *Cadence Design Systems, Inc., San Jose, CA*
Jae-Hyun Kang - *Samsung Electronics Co., Ltd. & Samsung Semiconductor, Inc., Yongin-si, Republic of Korea*
Byungchul Shin, Namjae Kim, Seungweon Paek, Byungmoo Song - *Samsung Electronics Co., Ltd. & Samsung Semiconductor, Inc., Gyeonggi-do, Republic of Korea*
Jac Condella, Philippe Hurat, Frank E. Gennari, Ya-Chieh Lai - *Cadence Design Systems, Inc., San Jose, CA*

7.5 A Methodology for ESD-CDM Oxide Failure Analysis & Prevention with Silicon correlation
Karthik Kodakandla, **Murali M. Thota** - *Texas Instruments India Pvt. Ltd., Bengaluru, India*
Nayan Chandak, Mathew J. Kaipanatu - *ANSYS, Inc., Bengaluru, India*

7.6 Graph Databases to Enable High Performance Microprocessor Design
Kerim Kalafala - *IBM Corp., Hopewell Junction, NY*
Anshul, Charles Gates, Ajay Gopalakrishnan, Ramadevi Kilaru, Prabhat Maurya, Haritha Mudimela, Shesha Raghunathan, Harrold Reindel, Richard Taggart - *IBM Corp., Poughkeepsie, NY*
Tom Guzowski - *IBM Corp., Essex, Vermont*

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DT8 DESIGNER TRACK: WHEN ACCURACY MEETS POWER: 2018 DAC SYSTEM DESIGN CONTEST ON LOW POWER OBJECT DETECTION

Time: 3:30 - 5:00pm || Room: 2010 || Event Type: Designer Track Invited
Keywords: Architecture & System Design, Low-Power & Reliability, Contests
Topic Area: Machine Learning/AI

CHAIR:
Bei Yu - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*

ORGANIZERS:
Yiyu Shi - *Univ. of Notre Dame, IN*
Jingtong Hu - *Univ. of Pittsburgh, PA*

This is a special session dedicated to the top three teams of the 2018 DAC System Design Contest on Low Power Object Detection. The contest has attracted over 120 teams from more than 10 countries/regions. All contestants have received a large training dataset provided by DJI, a company renowned for drone technologies. The dataset contains over 14 GB of images with 100 different objects to detect. A hidden dataset will be used to evaluate the performance of the designs in terms of accuracy and power. Contestants compete in two different categories: FPGA using Xilinx PYNQ-Z1 and GPU using Nvidia TK2, and a monthly ranking will start from January.

8.1 Introduction to 2018 DAC System Design Contest: Dataset, Statistics and Discoveries
Yiyu Shi - *Univ. of Notre Dame, IN*
Jingtong Hu - *Univ. of Pittsburgh, PA*
Cong Zhao - *DJI, Shenzhen, China*
Xiaowei Xu - *Univ. of Notre Dame, IN*
Xinyi Zhang - *Univ. of Pittsburgh, PA*

8.2 Third Place Winner Presentation: GPU Category

8.3 Second Place Winner Presentation: GPU Category

8.4 First Place Winner Presentation: GPU Category

8.5 Third Place Winner Presentation: FPGA Category

8.6 Second Place Winner Presentation: FPGA Category

8.7 First Place Winner Presentation: the FPGA Category

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IP9 IP TRACK: TEST AND YIELD ISSUES FOR IP IN COMPLEX SOCS

Time: 3:30 - 5:00pm || Room: 2008 || Event Type: IP Track Invited
Keywords: Test & Verification, Emerging Architectures & Technologies, Logic & High-Level Synthesis || Topic Area: IP, Design

CHAIR & ORGANIZER:
Henning Spruth - *NXP Semiconductors, Austin, TX*

Achieving good testability and yield is often considered a problem that needs to be addressed at the IP level. However, system complexity, a heterogeneous IP portfolio, new technology constraints and the need to balance die size, performance and test cost also make it necessary to look at this problem from a SoC architecture and IP integration point of view. The presentations in this session sample some of the angles from which the issue can be addressed.

9.1 Repair and Reliability Considerations for FinFET Memory IP
Raymond Leung - *Synopsys, Inc., Mountain View, CA*

9.2 Planning for Rapid IP Yield Ramp: Leveraging IJTAG for Third Party IP Integration, Silicon Bring up and Debug
Matt Knowles - *Mentor, A Siemens Business, Portland, OR*

9.3 "Smart" Yield Optimization Architecture and Trade-offs for Memories and Other Circuits
Carol Pyron - *NXP Semiconductors, Austin, TX*

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DESIGNER/IP TRACK POSTER NETWORKING RECEPTION

Time: 5:00 - 6:00pm || Room: Level 2 Exhibit Floor || Event Type: Designer and IP Track Poster || Keywords: Any || Topic Area: Design, IP

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Designer/IP Track Poster Session held Monday, June 25 from 5:00 to 6:00pm on Level 2 Exhibit Floor. Designer/IP Track reviewed presentations will be included in the poster session.

123.1 Electro-thermal Simulation for Analog Designs
Alex Samoylov, Andrei Pashkovich - *Silvaco, Inc., Santa Clara, CA*

123.2 Soft-IPs Protection using Chaotic Map-based Encryption
Khaled S. Mohamed - *Mentor, A Siemens Business, Cairo, Egypt*

123.3 High Quality Test with Efficient usage of Optimal Number of I/Os
Jaidev Shenoy, Kavitha Shankar, Balaji Upputuri, - *GLOBALFOUNDRIES, Bangalore, India*
Hardik Bhagat - *GLOBALFOUNDRIES, Bengaluru, India*

123.4 Novel and Configurable Circuit for Post-Silicon Measurement of Dynamic and Leakage Power of Sequential Circuits
Kushal Kamal - *GLOBALFOUNDRIES, Bengaluru, India*
Navin Bishnoi - *GLOBALFOUNDRIES, Bangalore, India*

123.5 Solving the Flash Incompatibility Issue
Mike Eftimakis, Samriti Sood - *Arm Ltd., Cambridge, United Kingdom*

123.6 System in Package Power Integrity Analysis of Large Scale FPGA
Shaan Awasthi, Anil Gundurao - *Intel Programmable Solutions Group, San Jose, CA*

123.7 More than UVM/RTL Simulations: Compelling need for Hybrid Verification-Validation for SOC Class FPGA Designs
Ajay Bhaskaran - *L3 Technologies, Camden, NJ*
John C. Frye - *Drexel Univ. & L3 Technologies, Camden, NJ*

123.8 Identifying and Fixing Power Leaks
Vishnu Kanwar, Vijay Tayal, Mohit Kumar , Manish Kumar, **Qazi Faheem Ahmed** - *Mentor Graphics (India) Pvt. Ltd., Noida, India*

123.9 Advantages and Pitfalls for Hierarchical CDC Analysis
Rohit K. Sinha - *Intel Technology India Pvt. Ltd, Bangalore, India*
Ping Yeung - *Mentor, A Siemens Business, Fremont, CA*

123.10 From how we Tackle NP-Complete to a new ECO Technique Applying Precise "Circuit Surgery"
Yu-Liang Wu, Xing Wei - *Easy-Logic Technology Limited, Hong Kong*

123.11 A Fast Library Evaluation Method based on Static Liberty Comparison
Senhua Dong - *Huada Empyrean Software Co., Ltd, Beijing, China*
Dingshan You - *Guizhou Huaxintong Semiconductor Technologies Co., Ltd & Huada Empyrean Software Co., Ltd, Beijing, China*
Ying Li - *Guizhou Huaxintong Semiconductor Technologies Co., Ltd, Beijing, China*
Xiao Yong - *Huada Empyrean Software Co., Ltd, Beijing, China*
Jamie Chen - *Huada Empyrean Software Co., Ltd, San Diego, CA*

123.12 Power Integrity of Large 3D ICs
Shashidhara S. Bapat - *Broadcom Limited, Bangalore, India*
Ruggero Castagnetti - *Broadcom Corp., San Jose, CA*

123.13 ISO 26262: How Safe is your Safety Mechanism?
Ping Yeung - *Mentor, A Siemens Business, Fremont, CA*
Abdelouahab Ayari - *Mentor, A Siemens Business, Munich, Germany*

123.14 Power-efficient Clock Tree Design
Shashank B. Sreekanta - *GLOBALFOUNDRIES, Bangalore, India*

123.15 Hybrid Chip-Level Power Analysis Flow in Mobile Design
Dajen Huang - *MediaTek, Inc., Sunnyvale, CA*
Ya-Shih Huang, Shang-Wei Tu, Peng-Chuan Huang - *MediaTek, Inc., Hsinchu, Taiwan*

123.16 Early Level Thermal Analysis and Thermal Aware Design Flow
Joohee Choung, Wook Kim, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Yonghwan Kim - *Samsung Electronics Co., Ltd., Seoul, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

123.17 Power and Reliability Analysis for Next Generation InFO & CoWoS Style Designs
Abhishek Chakraborty - *MediaTek, Inc., Bengaluru, India*
Rajeev Singh, Dravit Rana - *MediaTek, Inc., Bangalore, India*
Sankar Ramachandran - *ANSYS, Inc. & Apache Design, Inc., A Subsidiary of ANSYS, Inc., Bangalore, India*
Naveen Bapu, Ramesh Agarwal - *ANSYS, Inc., Bangalore, India*

123.18 A Generic, Fully Automated Physical Verification Methodology for 2.5D-IC
Kalyana Kumar A, Parthasarathy V - *Advanced Micro Devices, Inc., Bengaluru, India*
Zhang Zhao, Daniel Yingdong - *Advanced Micro Devices, Inc., Shanghai, China*
Bhavani Prasad - *Mentor, A Siemens Business, Bengaluru, India*
Tarek Ramadan - *Mentor, A Siemens Business, Cairo, Egypt*

123.19 Increased Productivity Solution for Full Custom Layout
Atul Bhargava, Komal Arora, Rajeev Singh - *STMicroelectronics, Greater Noida, India*
Vishesh Kumar - *Cadence Design Systems (India) Pvt. Ltd. & STMicroelectronics, NOIDA, India*
Eric Picollet - *STMicroelectronics, Crolles, France*

123.20 Improving Process Uniformity with CMP Aware Fill Insertion Technique
Yongfu Li - *GLOBALFOUNDRIES, Singapore*
Jiansheng Jansen Chee, **Tamba Gbondo-Tugbawa** - *Cadence Design Systems, Inc., San Jose, CA*
Ushasree Katakamsetty - *GLOBALFOUNDRIES, Singapore*
Sam Nakagawa - *GLOBALFOUNDRIES, Santa Clara, CA*
Brian Lee - *Cadence Design Systems, Inc., San Jose, CA*
Aaron Gower-Hall - *Cadence Design Systems, Inc., Santa Clara, CA*

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DESIGNER/IP TRACK POSTER SESSION

123.21 Static Timing Analysis Using NanoTime for Custom Circuits
Lily Aggarwal - *Microsoft Corporation, Mountain View, CA*

123.22 UVM VIP Framework for Verification of High-Speed Interface Rx Data-Path
Anil Deshpande, Arnab Ghosh, Ankit Garg, Somasunder Kattepura Sreenath - *Samsung Semiconductor India R&D, Bangalore, India*

123.23 Modeling Clocks, Resets and Power Rails in SoC Functional Simulator
Raghav Tenneti, **Praveen Wadikar**, Kamal Jeet - *NVIDIA Corp., Bangalore, India*

123.24 Low-resource Cryptography for Highly Constrained IoT Devices
Derek Atkins - *SecureRF Corporation, Shelton, CT*

123.25 Multi-cycle Path Exceptions Automation and Verification Methodology
Akshay A. Mote, Sandhya Sundaram, Joshua K. Carroll, Sudhanshu Salgiya - *Intel Corp., Folsom, CA*

123.26 Integrated ESD Solution: How Various ESD Checks can be Integrated in a Single Flow for Efficient Analysis
Abdullah Mansoor, Muhammad Ali - *Intel Corp., Hillsboro, OR*

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NETWORKING RECEPTION AND SILICON/TECHNOLOGY ART SHOW

Time: 6:00 - 7:00pm || Room: Level 2 Lobby || Event Type: Networking
Keywords: Any

Join attendees for refreshments and lively discussion and DAC's 2nd Silicon/Technology Art Show.

The Silicon/Technology Art Show will feature stunning images submitted by DAC attendees that demonstrate the beauty of everyday work in this industry. Submitted pieces will be judged in various categories and the winners for each category will be announced during the reception.

Awards include:

- Best Visualization
- Most Inspiring
- Most Insightful
- Most Artistic

Grand Prize- Best piece out of all categories.

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T1

TUTORIAL 1: MODEL-BASED DESIGN & SIMULATION TOOLS FOR HETEROGENEOUS AUTOMOTIVE HW/SW SYSTEMS

Time: 10:30am - 12:00pm || Room: 3016 || Event Type: Monday Tutorial
Keywords: Architecture & System Design, Test & Verification, Emerging Architectures & Technologies || Topic Area: Automotive, Design

ORGANIZERS:

Arne Hamann, - *Robert Bosch GmbH, Renningen, Germany*
Dirk Ziegenbein - *Robert Bosch GmbH, Renningen, Germany*

The future mobility will be electrified, automated and connected. As a result, automotive systems are currently undergoing a radical shift in the way they are organized and designed at the software and hardware levels, leading to a threefold heterogeneity:

1. Formerly separated function domains are integrated onto centralized computing platforms leading to a heterogeneous mix of applications with different models of computation
2. Hardware will be diverse and specialized to satisfy the tremendous increase of needed computing power
3. Collaborating parties for design and development will be more heterogeneous as compared to today

In this complex setup, design and simulation tools based on abstract models efficiently enable discussion and assessment across all development stages to achieve excellent HW/SW solutions. The tutorial is centered around AMALTHEA, the open source de-facto standard for performance modeling of automotive systems.

Bosch will highlight the current trends & challenges in automotive systems engineering that stem from the threefold heterogeneity, motivate the usage of system level design and simulation tools for increasing design efficiency, and introduce the AMALTHEA eco-system.

Silexica will present new design tools based on state-of-the-art compiler technology and full heterogeneous platform awareness. An AMALTHEA based approach of parallelization and software distribution will be demonstrated that is capable to perform automatic system-level performance estimation.

INCHRON will present a real-time simulation tool for heterogeneous multi-core systems. Based on a multi-sensor advanced driver assistance system modeled with AMALTHEA, two challenges are addressed: optimization of end-to-end latencies, and the impact of heavily loaded interconnects on system performance.

SPEAKERS:

Arne Hamann - *Robert Bosch GmbH, Renningen, Germany*
Maximilian Odendahl - *Silexica Software Solutions GmbH, Köln, Germany*
Helmar Wieland - *INCHRON GmbH, Potsdam, Germany*

T2

TUTORIAL 2: FUNCTIONAL SAFETY & RELIABILITY FOR AUTOMOTIVE APPLICATIONS

Time: 10:30am - 12:00pm || Room: 3018 || Event Type: Monday Tutorial
Keywords: Emerging Architectures & Technologies, Low-Power & Reliability, Test & Verification || Topic Area: Automotive, EDA

ORGANIZERS:

Alessandra Nardi - *Cadence Design Systems, Inc., San Jose, CA*
Viktor Preis - *Cadence Design Systems GmbH, Munich, Germany*
Christian Sauer - *Cadence Design Systems GmbH, Munich, Germany*

The race to self-driving cars is making the news almost daily. Legal, ethical and legislative implications aside, this new market is an incredibly fast driver for the evolution of SoC development for automotive applications. Advanced Driver Assistance Systems (ADAS), the precursor of fully autonomous vehicles, led to an exponential increase in the amount and complexity of electronics in cars. ADAS applications are computationally intensive and require advanced process nodes to meet the performance/watt needs. Safety-critical automotive applications have stringent demands for functional safety and reliability: these metrics are becoming an integral part of the semiconductor design flow.

The first part of the tutorial provides an overview of functional safety and reliability requirements for automotive applications and it introduces functional safety concepts as defined in the ISO 26262 standard to address random and systematic failures: ASIL (Automotive Safety Integrity Level), FMEDA (Failure Modes, Effects, and Diagnostic Analysis), Fault Classification and Tool Confidence Level (TCL). It then describes how functional safety integrates and drives the traditional design/verification/implementation flow for semiconductors. The second part dives into a detailed FMEDA use case and provides an overview of safety mechanisms typically required for different system components. Impact of failure modes and failure modes distribution on overall system ASIL metric is also discussed. The early FMEDA contains the diagnostic coverage values based on analysis, engineering judgment and reference to ISO 26262-5. The tutorial details, as for the final FMEDA release, the diagnostic coverage values are confirmed via safety verification, including simulation with fault injection.

SPEAKERS:

Alessandra Nardi - *Cadence Design Systems, Inc., San Jose, CA*
Sandeep Goel - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*

T3 TUTORIAL 3: HARNESSING DATA SCIENCE FOR THE HW VERIFICATION PROCESS

Time: 10:30am - 12:00pm || Room: 3020 || Event Type: Monday Tutorial
Keywords: Test & Verification || Topic Area: EDA, Machine Learning/AI

ORGANIZERS:

Raviv Gal, Avi Ziv - *IBM Research - Haifa, Israel*

Modern verification is a highly automated process that involves many tools and subsystems. These verification tools produce large amount of data that is essential for understanding the state of the verification process. The growing amount of data the verification process produces, and the complex relations between verification tools calls for data science techniques such as statistics, data visualization, and machine learning to extract the essence of the data and present it to the users in a simple and clear manner.

The goal of the tutorial is to teach the audience how to harness the powers of data science into tools that improve the verification process and assist in understanding and managing it. The tutorial begins with a brief overview of the challenges and benefits of building a system that stores, processes and analyzes the verification data of verification projects. We then describe various components and aspects in such a system. The main focus of the tutorial is on specific analysis techniques that are accompanied by concrete examples. In that sense, the tutorial sheds light on the application of advanced data analysis techniques in many steps of the verification cycle, such as accelerating coverage data analysis, estimating formal verification effort, and anomaly detection in post-silicon validation. We conclude with open research problems that can lead to the "holy grail" of cognitive verification.

The tutorial uses real life examples from the IBM Verification Cockpit, a platform for collecting and analyzing verification data and Mentor Graphics state-of-the-art functional verification solutions.

SPEAKERS:

Avi Ziv - *IBM Research - Haifa, Israel*
Eman El Mandouh - *Mentor, A Siemens Business, Cairo, Egypt*

T4 TUTORIAL 4: DESIGNING IN ADVANCED TECHNOLOGIES: A QUICK REVIEW OF APPROACHES

Time: 10:30am - 12:00pm || Room: 3022 || Event Type: Monday Tutorial
Keywords: Physical Design & DFM, Interconnects || Topic Area: Design, EDA

ORGANIZER:

Puneet Gupta - *Univ. of California, Los Angeles, CA*

This tutorial will cover topics relating to design in advanced semiconductor technology nodes, especially, 14nm and 10nm.

We will start with a brief introduction on FinFET and highlight PPA scaling from planar devices to FinFET 14nm, 10nm, and 7nm. Then, we will explain key properties of FinFET and its impact on chip design. For example, steep subthreshold slope together with fully depleted channel in FinFET has improved leakage and its variation. This enables aggressive voltage scaling and high Vt cell usage for power reduction. Meanwhile, FinFET has more design constraints (e.g., discretized fins in standard cell design). We will discuss how these constraints can be overcome by innovative technology and design co-optimizations for PPA improvements.

The process technology scaling from planar-device-based nodes to FinFET-based nodes was accompanied by a transition in the interconnect patterning to multiple-patterning. For first generation FinFET nodes, that transition started in the local, short-range interconnects for both the "middle-of-line (MOL)" layers and minimum-pitch "back-end-of-line (BEOL)" layers. Since then, it has proliferated up the BEOL stack. At the same time, the primarily copper-based MOL and lower-level BEOL layers have also hit an inflection point in resistivity (versus line-width), leading to an exponential increase in cost and design complexity needed to overcome the constraints imposed by multiple patterning and the electrical effects imposed by the disproportionate increase in interconnect parasitics. This tutorial will go over the impact of interconnect scaling and design solutions needed to overcome the various constraints and limitations.

SPEAKERS:

Tuck-Boon Chan - *Qualcomm, Inc., Los Angeles, CA*
Jim Dodrill - *Arm Ltd., Austin, TX*

T5

TUTORIAL 5: UTILIZING THE TALENTS OF YOUR TEAMS (PART 1): THE SECRET TO MAKE YOUR TEAM HIGH PERFORMING

Time: 10:30am - 12:00pm || Room: 3024 || Event Type: Monday Tutorial
Keywords: Any || Topic Area: Design, EDA

ORGANIZERS:

Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Laleh Behjat - *Univ. of Calgary, Canada*
Patrick Haspel - *Cadence Design Systems, Inc., San Francisco, CA*

Check out Tutorial 10 for Part 2!

In this interactive tutorial, we will give you practical tools you can use to turn your team into a high-performing one. A high-performing team can achieve one hundred percent of expected results of a task and find new and innovative ways for the future. The session starts with an overview of the definition of high-performing teams. Then, we will take part in a role-playing exercise. Through this exercise, we will see how our interactions and implicit biases can hinder or improve the performance of our teams. Finally, we will give you a toolbox of practical solutions. We will show you how to use this toolbox to improve your team's performance.

The topics covered in this tutorial are applicable industry, academics and students. We are hoping that by using the toolkit offered in this workshop, your team can find better solutions to today's challenging EDA problems.

SPEAKERS:

Laleh Behjat - *Univ. of Calgary, Canada*
Patrick Haspel - *Cadence Design Systems, Inc., San Jose, CA*

T6

TUTORIAL 6: EMBEDDED MACHINE LEARNING IN THE INTERNET OF THINGS

Time: 1:30 - 5:00pm || Room: 3016 || Event Type: Monday Tutorial || Keywords: Emerging Architectures & Technologies, Architecture & System Design, Low-Power & Reliability || Topic Area: IoT, Machine Learning/AI

ORGANIZER:

Robert Dick - *Univ. of Michigan, Ann Arbor, MI*

Shortly, every human will be served by hundreds or thousands of sensing, decision making, and actuating machines. These smart things will be connected to each other, and the rest of the world, but for the many that operate on battery power, communication will impose severe energy consumption penalties. Local computation will need to convert sparse data to dense information and many decisions will be made locally. This implies new approaches to the design of machine learning algorithms and hardware, in which energy efficiency joins accuracy as a central optimization objective, and the communication and computation implications of partitioning machine learning algorithm components among embedded systems and higher-performance servers must be explicitly considered.

This tutorial will cover recent developments in IoT machine learning systems including new applications and methods of constructing and using system models. These developments span the network, from edge to cloud. In addition, we will describe specific algorithmic and hardware developments enabling advances at each level: from edge, to network, to cloud. For example, we will describe neural network compression techniques appropriate for operation in resource-constrained environments near the edge of the network. Custom and semi-custom hardware architecture designed specifically for deeply embedded machine learning will be described, and the differences between architectures appropriate for edge and cloud will be contrasted. Each speaker has published novel research in the area or developed commercial products that overcame the challenges peculiar to the embedded machine learning domain.

SPEAKERS:

Bo Wu - *Google, Inc., Mountain View, CA*
Li Shang - *Univ. of Colorado, Boulder, CO*
Tajana Simunic Rosing - *Univ. of California, San Diego, La Jolla, CA*
Hun Seok Kim - *Univ. of Michigan, Ann Arbor, MI*

T7 TUTORIAL 7: SECURITY OF INTERNET OF THINGS (IOT) AND CYBER-PHYSICAL SYSTEMS (CPS): A HANDS ON APPROACH

Time: 1:30 - 5:00pm || Room: 3018 || Event Type: Monday Tutorial || Keywords: Architecture & System Design, Test & Verification || Topic Area: IoT, Security/Privacy

ORGANIZERS:

Yier Jin - *Univ. of Florida, Gainesville, FL*
Mark Tehranipoor - *Univ. of Florida, Gainesville, FL*
Vivek De - *Intel Corp., Hillsboro, OR*

Internet of Things (IoT) have become prevalent in every day life. Harmless as it may seem, this new breed of devices have raised a number of privacy and security concerns. Security issues may come at different levels, from deployment issues that leave devices exposed to the internet with default credentials, to implementation issues where manufacturers incorrectly employ existing protocols or develop proprietary ones for communications that have not been examined for their sanity. On the hardware side, a device may also be vulnerable. An attacker with physical access to a device may be able to alter its functionality. Meanwhile, cyber-physical systems (CPS) comprise the backbone of national critical infrastructures such as power grids, transportation systems, home automation systems, etc. Because cyber-physical systems are widely used in these applications, the security considerations of these systems should be of very high importance. We will provide detailed examples of our experimentation with CPS devices. We will then present solutions that have been proposed by both industry and academia. Besides the introduction to the IoT and CPS security, hands-on labs are also prepared for all audience. Commercial smart devices (web cams) will be provided where audiences can practice on how to identify security vulnerabilities of modern connected smart devices as well as how to exploit these vulnerabilities. The performed hands-on labs will cover hardware attacks, device authentication, remote access, and MITM attacks. Potential solutions to secure these devices will also be discussed in the hands-on labs.

SPEAKERS:

Yier Jin - *Univ. of Florida, Gainesville, FL*
Xinwen Fu - *Univ. of Central Florida, Orlando, FL*

T8 TUTORIAL 8: MACHINE LEARNING FOR EDA APPLICATIONS

Time: 1:30 - 5:00pm || Room: 3020 || Event Type: Monday Tutorial || Keywords: Emerging Architectures & Technologies, Any || Topic Area: Machine Learning/AI, EDA

ORGANIZER:

Manish Pandey - *Synopsys, Inc., Mountain View, CA*

This tutorial covers machine learning algorithms and application methodologies necessary for building EDA applications and flows. We start with supervised machine learning algorithms, which create models from labeled training data sets. However, the clear majority of data generated by EDA tools and flows today are not labeled, which precludes supervised learning. Yet, there is significant value can be derived from these data sets, including understanding of the structure of data using clustering and similarity analysis, discovery of hidden underlying probability distributions, all of which can lead to better design of algorithms, failure analysis, and new data and feature insights. We discuss several unsupervised learning algorithms that make this possible. We also discuss some recent machine learning advances such as Generative Adversarial Networks which learn underlying data distributions without labels. Another class of problems we discuss involves systems or software agents that take actions in an environment to maximize some notion of cumulative reward. The problems in this class range from autonomous driving to driving randomized simulation for better coverage, to smart place and route algorithms.

The second part of the tutorial focuses on the more practical aspects of applying different algorithms to solve classical EDA problems. Solving production problems within electronic design automation is complex. Production engineering applications have accuracy, scalability, complexity, verifiability, and usability requirements that are not met by traditional machine learning approaches. These additional challenges frequently cause production machine learning approaches to fail. The presentation covers these engineering-specific challenges and presents some effective solutions.

SPEAKERS:

Manish Pandey - *Synopsys, Inc., Mountain View, CA*
Claudionor Coelho - *Google, Inc., Mountain View, CA*
Jeff Dyck - *Mentor, A Siemens Business, SK, Canada*

T9 TUTORIAL 9: DESIGN TOOLS FOR VERIFYING HARDWARE SECURITY

Time: 1:30 - 5:00pm || Room: 3022 || Event Type: Monday Tutorial
Keywords: Test & Verification || Topic Area: Security/Privacy

ORGANIZERS:

Ryan Kastner - *Univ. of California, San Diego, La Jolla, CA*
Wei Hu - *Northwestern Polytechnical Univ., Xi'an, China*

Hardware security vulnerabilities are notoriously hard to detect and even more difficult to fix after fabrication. Unfortunately, state-of-the-art secure hardware design process still heavily relies on manual inspection to determine if the design is free of any and every security vulnerability. Hardware designers and verification engineers are in desperate need of tools and techniques to enable deeper and more complete security analysis. In this tutorial, we describe how emerging hardware security verification tools help fill this need. The presentations bridge from theory to practice with the goal of exposing attendees to the latest research while demonstrating the practicality of these techniques to test and verify a variety of different security properties on real hardware designs through security verification.

The 3-hour long tutorial has four expert speakers to present the most recent advances in hardware security verification techniques and tools. There is a focus on how to practically use these tools to secure different parts of the system design including digital hardware and firmware. We start with a session that covers the foundations of hardware security verification (Prof. Tim Sherwood, UC Santa Barbara). Then, we will dive into more details about some of the most prevalent hardware security verification tools; these include SecVerilog/Secure Chisel for processor design (Prof. G. Edward Suh, Cornell), proof carrying hardware for IP protection and analog designs (Prof. Yiorgos Makris, UT Dallas), and utilizing hardware security tools "in the wild" to verify security properties on state of the art hardware designs (Dr. Jason Oberg, Tortuga Logic).

SPEAKERS:

Tim Sherwood - *Univ. of California, Santa Barbara, CA*
G. Edward Suh - *Cornell Univ., Ithaca, NY*
Yiorgos Makris - *Univ. of Texas at Dallas, TX*
Jason Oberg - *Tortuga Logic, San Jose, CA*

T10 TUTORIAL 10: UTILIZING THE TALENTS OF YOUR TEAMS (PART 2): BIAS BUSTERS @DAC

Time: 1:30 - 5:00pm || Room: 3024 || Event Type: Monday Tutorial
Keywords: General

ORGANIZERS:

Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Laleh Behjat - *Univ. of Calgary, AB, Canada*
Patrick Haspel - *Cadence Design Systems, Inc., San Jose, CA*

Check out Tutorial 5 for Part 1!

Do you make your decisions based on logic or are there outside influences that affect your actions and decisions? Implicit bias is unconscious thinking that influences our understanding of our world and how we interact with it. Everyone has implicit or unconscious biases, and because they are unconscious, we are unaware of them. These biases are believed to be a contributing factor that has stalled efforts at increasing diversity. In this tutorial, the basis of implicit bias is discussed and tools for awareness and mitigation of its unwanted effects are provided. The session is meant for bystanders who can intervene when they see implicit bias in others.

The first part of this tutorial presents current understanding of what unconscious bias is, and how we can reduce their impacts. The second part of the tutorial is intended for attendees who want to take the Bias Busters program back to their institutions.

Bias Busters @ Work (BB@Work) was created by Google as an extension of the Unconscious Bias @ Work Workshop (UB@Work), a course aimed at raising awareness of how unconscious biases work, how they can negatively influence workplace interactions, and what tools can help disrupt bias. In 2015, Google and Carnegie Mellon University created the Bias Busters @ University program. More information on Bias Busters @ Work: https://rework.withgoogle.com/subjects/unbiasing/.

This session is designed for academics and industry participants. We hope that through this session, you will be able to make more diverse and inclusive teams and increase your performance.

SPEAKERS:

Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Gerry Katilius - *Google, Inc., Pittsburgh, PA*
Jonathan Reynolds - *Carnegie Mellon Univ., Pittsburgh, PA*

OPENING SESSION & AWARDS PRESENTATION

Time: 9:00 - 9:20am || Room: 3008

DAC's Executive Committee will highlight the conference's events, and the award presentations will recognize success and excellence for individuals in the field of design automation of electronic systems.

IEEE CEDA OUTSTANDING SERVICE AWARD

Michael 'Mac' McNamara, Adapt-IP
For outstanding service to the EDA community as DAC General Chair in 2017.

Vijaykrishnan Narayanan, Pennsylvania State University
For his outstanding 4-year service as Editor-in-Chief (EiC) for the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).

IEEE FELLOW

Yiran Chen, Duke University
For contributions to spintronic memory.

IEEE FELLOW

Zhuo Li, Cadence Design Systems, Inc.
For contributions to physical synthesis and modeling of integrated circuits.

IEEE FELLOW

Sanjit A. Seshia, University of California, Berkeley
For contributions to formal methods for inductive synthesis and algorithmic verification.

IEEE FELLOW

Mark M. Tehranipoor, University of Florida
For contributions to integrated circuits security and trust.

IEEE FELLOW

Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg
For contributions to hardware/software co-design for embedded systems.

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

Luca Amarú, Pierre-Emmanuel Gaillardon, Giovanni De Micheli
Majority-Inverter Graph: A New Paradigm for Logic Optimization," Vol. 35, Issue 5, pp. 806 – 819, May 2016.

ACM SIGDA PIONEER AWARD

Mary Jane Irwin - *Pennsylvania State University*
For contributions to VLSI architectures, electronic design automation and community membership.

2018 ACM TODAES BEST PAPER AWARD

Kan Xiao, Domenic Forte, Yier Jin, Ramesh Karri, Swarup Bhunia, Mark M. Tehranipoor
"Hardware Trojans: Lessons Learned after One Decade of Research," ACM TODAES Volume 22 Issue 1, December 2016, Article No. 6.

ACM SIGDA DISTINGUISHED SERVICE AWARD

Chuck Alpert, Cadence Design Systems
For significant contributions to DAC.

Jörg Henkel, Karlsruhe Institute of Technology
For leading SIGDA efforts in Europe and DATE.

Michael 'Mac' McNamara, Adapt-IP
For sustained contributions to the design automation community and DAC.

Michelle Clancy, Cayenne Communication
For sustained contributions to the community, especially DAC.

ACM SIGDA OUTSTANDING NEW FACULTY AWARD

Shimeng Yu, Arizona State University

ACM SIGDA OUTSTANDING PH.D. DISSERTATION AWARD

Xiaoqing Xu – "Standard Cell Optimization and Physical Design in Advanced Technology Nodes"
Advisor: David Pan

Pramod Subramanyan – "Deriving Abstractions to Address Hardware Platform Security Challenges"
Advisor: Sharad Malik

ACM FELLOW

Martin Wong - *University of Illinois Urbana-Champaign*
For contributions to the algorithmic aspects of electronic design automation (EDA).

KEYNOTE: THE FUTURE OF COMPUTING: PUSHING THE LIMITS OF PHYSICS, ARCHITECTURES & SYSTEMS FOR AI

DARIO GIL – *Vice President of AI and IBM Q, IBM Research, Yorktown Heights, NY*

Time: 9:20 - 10:00am || Room: 3008 || Keywords: Architecture & System Design, Emerging Architectures & Technologies
Topic Area: Machine Learning/AI

The extraordinary progress in AI over the last few years has been enabled, in part, by modern advancements in computing. Algorithmic ideas that had been around for decades have finally been brought to life thanks to Moore's Law and innovations in microprocessor and computing architectures. As Moore's Law slows and data volumes explode we can expect to see new types of innovations emerge that will allow the rate of progress to continue. My presentation will cover state-of-the art computing for AI, as it exists today, as well as a roadmap of innovations that will lead us into the decade(s) to come. This includes the importance of approximate computing (both algorithms and hardware), analog devices for AI, and quantum computing for AI. I will also highlight how these innovations bring forth both challenges and unique opportunities for the design automation community.

Biography: Dr. Gil is a leading technologist and senior executive at IBM. As Vice President of AI and IBM Q, Dr. Gil is responsible for IBM's artificial intelligence research efforts and for IBM's commercial quantum computing program (IBM Q). Prior to his current position Dr. Gil was the VP of Science and Solutions, directing a global organization of 1,500 researchers across 12 laboratories with a broad portfolio of activities spanning the physical sciences, the mathematical sciences, and industry solutions based on AI, IoT, blockchain and quantum technologies. His research results have appeared in over 20 international journals and conferences, he is the author of numerous patents. Dr. Gil is an elected member of the IBM Academy of Technology. He received his Ph.D. in Electrical Engineering and Computer Science from MIT.

10 DEEP SECURE THOUGHTS

Time: 10:30am - 12:00pm || Room: 3014 || Event Type: Research Reviewed
Keywords: Any || Topic Area: Security/Privacy

CHAIR:
Christopher Harris - *Auburn Univ., Auburn, AL*

CO-CHAIR:
Ro Cammarota - *Qualcomm Research, San Diego, CA*

A series of research projects are presented which employ deep learning to achieve security. Learning is used to recognize malware execution, enable private distributed collaboration, and perform approximate decryption. Learning systems are protected from side-channel attack via memory address access patterns.

10.1 Ensemble Learning for Effective Run-Time Hardware-Based Malware Detection: A Comprehensive Analysis and Classification
Hossein Sayadi - *George Mason Univ., Fairfax, VA*
Nisarg Patel - *ASML & George Mason Univ., Wilton, CT*
Sai Manoj Pudukotai Dinakarrao, Avesta Sasan, Setareh Rafatirad, Houman Homayoun - *George Mason Univ., Fairfax, VA*

10.2 DeepSecure: Scalable Provably-Secure Deep Learning
Bita Darvish Rouhani - *Univ. of California, San Diego, La Jolla, CA*
M. Sadegh Riazi - *Univ. of California, San Francisco, CA*
Farinaz Koushanfar - *Univ. of California, San Diego, La Jolla, CA*

10.3 DWE: Decrypting Learning with Errors with Errors
Song Bian, Masayuki Hiromoto, Takashi Sato - *Kyoto Univ., Kyoto, Japan*

10.4 Reverse Engineering Convolutional Neural Networks Through Side-channel Information Leaks
Weizhe Hua, Zhiru Zhang, G. Edward Suh - *Cornell Univ., Ithaca, NY*

11 HOW SOLID IS YOUR STORAGE?

Time: 10:30am - 12:00pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Architecture & System Design || Topic Area: ESS

CHAIR:
Jingtong Hu - *Univ. of Pittsburgh, PA*

CO-CHAIR:
Rangharajan Venkatesan - *NVIDIA Corp., Santa Clara, CA*

Solid State Drives (SSDs) are the mainstay of computing platforms at various scales. This session focuses on enhancing the performance of SSDs and file systems. First, performance enhancements for journaling file systems are addressed. Next, write amplification to boost performance for non-volatile main memory file systems is explored. Lastly, techniques to improve garbage collection for SSDs are proposed.

11.1 OFTL: Ordering-Aware FTL for Maximizing Performance of the Journaling File System
Daekyu Park - *Sungkyunkwan Univ. & Samsung Electronics Co., Ltd., Gyeonggi-do, Republic of Korea*
Dong Hyun Kang, Young Ik Eom - *Sungkyunkwan Univ., Suwon, Republic of Korea*

11.2 LAWN: Boosting the Performance of NVMM File System through Reducing Write Amplification
Chundong Wang, Sudipta Chattopadhyay - *Singapore University of Technology and Design, Singapore*

11.3 FastGC: Accelerate Garbage Collection via an Efficient Copyback-Based Data Migration in SSDs
Fei Wu, **Jiaona Zhou**, Shunzhuo Wang, Yajuan Du - *Huazhong Univ. of Science & Technology & City Univ. of Hong Kong, Wuhan, China*
Chengmo Yang - *Univ. of Delaware, Newark, DE*
Changsheng Xie - *Huazhong Univ. of Science & Technology & Wuhan National Laboratory for Optoelectronics, Wuhan, China*

11.4 Dynamic Management of Key States for Reinforcement Learning-Assisted Garbage Collection to Reduce Long Tail Latency in SSD
Wonkyung Kang, Sungjoo Yoo - *Seoul National Univ., Seoul, Republic of Korea*

12 RE-INNOVATING THE ANALOG & MIXED-SIGNAL WORLD!

Time: 10:30am - 12:00pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Analog & Mixed-signal Design, Physical Design & DFM
Topic Area: EDA, Design

CHAIR:
Scott Little - *Maxim Integrated, Beaverton, OR*

CO-CHAIR:
Markus Olbrich - *Leibniz Univ. Hannover, Germany*

This session covers a broad range of technology advancements in analog, mixed-signal, and RF design, including layout, optimization, and calibration. The first paper introduces a new topological representation for analog layout design. The second paper deals with analog placement, integrating current flow and symmetry constraints. The third paper presents multi-objective Bayesian optimization for synthesis of analog/RF circuits, and the final paper proposes to design analog neural network processors by calibrating process variations with transfer learning.

12.1 WB-Trees: A Topological Representation for FinFET-Based Analog Layout Designs
Yu-Sheng Lu, Yu-Hsuan Chang, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

12.2 Analog Placement with Current Flow and Symmetry Constraints using PCP-SP
Abhishek Patyal, Po-Cheng Pan, Asha K A, Hung-Ming Chen - *National Chiao Tung Univ., Hsinchu, Taiwan*
Hao-Yu Chi, Chien-Nan Liu - *National Central Univ., Taoyuan, Taiwan*

12.3 Multi-Objective Bayesian Optimization for Analog/RF Circuit Synthesis
Wenlong Lyu, Fan Yang, Changhao Yan, Dian Zhou, Xuan Zeng - *Fudan Univ., Shanghai, China*
Wei Cai - *Fudan Univ., Dallas, TX*

12.4 Calibrating Process Variation at System Level with In-Situ Low-Precision Transfer Learning for Analog Neural Network Processors
Kaige Jia, Zheyu Liu, Qi Wei, **Fei Qiao**, Xinjun Liu, Yi Yang - *Tsinghua Univ., Beijing, China*
Hua Fan - *Univ. of Electronic Science and Technology of China, Chengdu, China*
Huazhong Yang - *Tsinghua Univ., Beijing, China*

13 SPECIAL SESSION: NEGATIVE CAPACITANCE FIELD EFFECT TRANSISTORS (NCFET) FOR ULTRA-LOW-POWER DEVICES TO SYSTEMS (EDA)

Time: 10:30am - 12:00pm || Room: 3020 || Event Type: Special Session
Keywords: Emerging Architectures & Technologies, Any, Architecture & System Design
Topic Area: EDA, Design

CHAIR:
Wilman Tsai - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*

ORGANIZERS:
Asif Khan, Sung-Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

Steep-slope transistors are emerging technologies that can further down-scale the power supply voltage and energy, and negative capacitance FET (NCFET)—a new type of transistor based on ferroelectric gate-oxides—has been shown to be one of the most promising steep-slope transistors through industry practices and system design. This session will give an overview of this technology with an emphasis on cross-layer interactions between device, circuit-system and application-level aspects.

The session will start with Sayeef Salahuddin (Berkeley) who will introduce the concept of NCFETs. What makes NCFETs particularly amenable to industry adoption is the CMOS-compatibility of "break-through" ferroelectrics. Zoran Krivokapic (GLOBALFOUNDRIES) will talk about how these oxides can enable NCFETs at advanced nodes and what the integration challenges are in light of their recent demonstration of high performance, state-of-the-art 14 nm node, negative capacitance FinFETs. Suman Datta (Notre Dame) will discuss circuit- and system-level aspects of NCFETs and related technologies.

13.1 Negative Capacitance Transistors
Sayeef Salahuddin - *Univ. of California, Berkeley, CA*

13.2 Negative Capacitance FETs and Other Ferroelectric Devices in Advanced Technology Nodes
Zoran Krivokapic - *GLOBALFOUNDRIES, Santa Clara, CA*

13.3 Beyond Logic Applications for Ferroelectric Negative Capacitance FETs
Suman Datta - *Univ. of Notre Dame, Notre Dame, IN*

14 CONFIGURE TO CONQUER: DYNAMIC HW/SW RECONFIGURATION FOR DEEP LEARNING

Time: 10:30am - 12:00pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Reconfigurable Systems, Architecture & System Design, Low-Power & Reliability || Topic Area: Machine Learning/AI, Design

CHAIR:
Priyanka Raina - *NVIDIA Corp., San Jose, CA*

CO-CHAIR:
Jae-sun Seo - *Arizona State Univ., Tempe, AZ*

The papers in this session have a common theme in that they propose to dynamically reconfigure DNN accelerators to improve their efficiency. The first paper dynamically scales the precision of computations. The second paper proposes to reconfigure the micro-architectural parameters of a neural network accelerator. The third paper reconfigures in software by changing the data-flow used for computation. The final paper dynamically partitions resources on reconfigurable platforms for modern deep neural network topologies like Inception and residual networks.

14.1 DPS: Dynamic Precision Scaling for Stochastic Computing-Based Deep Neural Networks
Hyeonuk Sim, Saken Kenzhegulov, Jongeun Lee - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*

14.2 DyHard-DNN: Even More DNN Acceleration With Dynamic Hardware Reconfiguration
Mateja Putic - *Univ. of Virginia, Charlottesville, VA*
Swagath Venkataramani, Schuyler Eldridge, Alper Buyuktosunoglu - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Mircea Stan - *Univ. of Virginia, Charlottesville, VA*
Pradip Bose - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

14.3 Exploring the Programmability for Deep Learning Processors: from Architecture to Tensorization
Chixiao Chen, Huwan Peng, Xindi Liu, Hongwei Ding, C.-J. Richard Shi - *Univ. of Washington, Seattle, WA*

14.4 LCP: Layer Clusters Paralleling Mapping Mechanism for Accelerating Inception and Residual Networks on FPGA
Xinhan Lin, Shouyi Yin, Fengbin Tu, Leibo Liu, Xiangyu Li, Shaojun Wei - *Tsinghua Univ., Beijing, China*

15 SPECIAL SESSION: MEMORY-CENTRIC ARCHITECTURES: INDUSTRY PERSPECTIVE FROM EMBEDDED SYSTEMS TO HIGH PERFORMANCE COMPUTING

Time: 10:30am - 12:00pm || Room: 3024 || Event Type: Special Session
Keywords: Architecture & System Design || Topic Area: Design

CHAIR & ORGANIZER:
John Kim - *KAIST, Daejeon, Republic of Korea*

For the past 50 years, systems architecture has mostly focused on feeding data to the processing units, including CPUs and GPUs, and the memory hierarchy have focused on allowing slow memory to work with fast processors. As Moore's Law slows down, faster processors do not continue to provide improved system performance. Instead, memory-centric architectures flip the existing model by bring the processing to the data, thereby reducing latency, lowering system power, and improving throughput. These architectures require rethinking all aspects of existing memory systems, from physical structures to workloads. Memory-centric organization is not only applicable for high-performance computing but also embedded and mobile systems. In this special session, we will have three invited speakers from the industry to discuss the impact of memory-centric architectures on different systems; talks will cover mobile workloads and their impact on mobile systems, near-data processing and accelerators, as well as high-performance computing and energy-efficient DRAM.

15.1 Memory Characterization for Mobile Workloads
Daehyun Kim - *Samsung Electronics America, Inc., Seoul, Republic of Korea*

15.2 Memory-centric Accelerators in High-performance Systems
Nuwan Jayasena - *Advanced Micro Devices, Inc., Santa Clara, CA*

15.3 Energy-Efficient DRAM for High-bandwidth Applications
Mike O'Connor - *NVIDIA Corp., Austin, TX*

DT16 DESIGNER TRACK: HACK@DAC: TECHNIQUES FOR FINDING SECURITY VULNERABILITIES IN AN SOC

Time: 10:30am - 12:00pm || Room: 2012 || Event Type: Designer Track Invited
Keywords: Test & Verification, Contests || Topic Area: Security/Privacy, EDA

CHAIR:
Jeyavijayan (JV) Rajendran - *Texas A&M Univ., College Station, TX*

CO-CHAIR:
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

ORGANIZERS:
Jeyavijayan (JV) Rajendran - *Texas A&M Univ., College Station, TX*
Daniel Holcomb - *Univ. of Massachusetts, Amherst, MA*
Siddharth Garg - *New York Univ., New York, NY*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

This session will present a set of novel approaches for discovering security vulnerabilities in SoC designs. System-on-a-Chip (SoC) designers use third-party or in-house intellectual property cores to design SOCs. Trustworthiness of such SoCs is undermined by security-critical bugs in IPs or integration. When exploited, a bug may result in a deadlock or failure of the system or create a backdoor allowing the attacker to gain remote access to the system so as to leak secrets from it. The research community has struggled with the problem of developing approaches and computer-aided tools to design trust-worthy SoCs.

The talks in this special session will present technical details of SoC security-enhancement techniques that have been evaluated against a common set of industry-provided benchmark designs in the 2018 Hack@DAC security competition. Hack@DAC includes a live one-day hacking competition at the conference where these techniques will be applied in a live-scoring capture-the-flag type event.

16.1 A Buggy SoC Framework for Security Assurance Research – Hack@DAC 2018 Case Study
Arun Kanuparthi, Hareesh Khattri - *Intel Corp., Hillsboro, OR*

16.2 Finalist team 1 from 2018 Hack@DAC presents their approach – Hackin' Aggies
Michael Quinn, Sheena Goel, Zhiyang Ong, Saumil Gogri, Bhavani Bedre Shankar - *Texas A&M Univ., College Station, TX*

16.3 Finalist team 2 from 2018 Hack@DAC presents their approach – TRELA
Yiorgos Makris, Mohammad-Mahdi Bidmeshki, Liwei Zhou, Monir Zaman, Yunjie Zhang - *Univ. of Texas at Dallas, Richardson, TX*

16.4 Finalist team 3 from 2018 Hack@DAC presents their approach – TPTSIC
Sumanta Chaudhuri, Michael Timbert - *Télécom ParisTech, Paris, France*
Xuan Thuy Ngo - *Secure-IC SAS, Paris, France*
Sylvain Guilley -*Télécom ParisTech, Paris, France*

16.5 Finalist team 4 from 2018 Hack@DAC presents their approach – Dallas Bugboys
Benjamin Carrion Schaefer, Siyuan Xu, Jianqi Chen - *Univ. of Texas at Dallas, Richardson, TX*

DT17 DESIGNER TRACK: MINDFULNESS: KEYS TO GOOD DESIGNER TIMES

Time: 10:30am - 12:00pm || Room: 2010 || Event Type: Designer Track Reviewed
Keywords: Physical Design & DFM || Topic Area: Design, EDA

CHAIR:
Parvesh Chapra - *GLOBALFOUNDRIES, Bengaluru, India*

Increasing design complexity requires a variety of insights into helping navigate design models, closure techniques and improving sign-off for reliability. Attend to find how to mine the secrets of time and achieve harmony between specifications and schedules. End the session by discharging your electrostatic build up!

17.1 Fast Timing Data Analysis for Better Performance, Power and Area on High Performance Computing Design
Yang Liu, Ping Liao - *HiSilicon, Chengdu, China*
Xiao Yong, Senhua Dong - *Huada Empyrean Software Co., Ltd, Beijing, China*

17.2 A Divergence Engine: Early Prediction of Clock-tree Divergence at Logic-synthesis Stage
Sanjana Sundaresh, **Murali Mohan Thota** - *Texas Instruments India Pvt. Ltd., Bengaluru, India*
Atul Garg - *Texas Instruments India Pvt. Ltd., Bangalore, India*

17.3 Load-aware Assertion Generation for Sub-blocks in Hierarchical Timing Optimization and Sign-off
Debjit Sinha - *IBM Corp., Poughkeepsie, NY*
Ravi C. Ledalla - *IBM Systems and Technology Group, Hopewell Junction, NY*
Chaobo Li, Tsz-mei Ko, Adil Bhanji, Hemlata Gupta - *IBM Corp., Poughkeepsie, NY*

17.4 Clock-level Scheduling Technique for Lowering Dynamic Voltage Drop Hot-spot
Jaewon Lee, Sangdo Park, Hyung-Ock Kim, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

17.5 Asymmetric Aging Timing Check in SOC
Yongsheng Sun - *HiSilicon, Chengdu, China*
Canhui Zhan - *HiSilicon, Shenzhen, China*
Joao Geada - *ANSYS, Inc., Concord, MA*
Jingbo Chen, Heyong Wu - *HiSilicon, Chengdu, China*
Zhenghao Gan, Waisum Wong - *HiSilicon, Shanghai, China*
Yu Xia - *HiSilicon, Shenzhen, China*

17.6 Dynamic ESD Analysis for Design Optimization and ESD Sign-off
Muhammad Ali, Tejas Tapsale - *Intel Corp., Hillsboro, OR*

IP18 IP TRACK: IP AND ARCHITECTURES FOR CMOS IMAGER SENSORS

Time: 10:30am - 12:00pm || Room: 2008 || Event Type: IP Track Invited
Keywords: Emerging Architectures & Technologies, Analog & Mixed-signal Design, Architecture & System Design || Topic Area: IP, Design

CHAIR & ORGANIZER:

Eric Esteve - *IP-nest, Nice, France*

The CMOS Image Sensor (CIS) market is one of the fastest growing semiconductor segments, with 10% annual growth. This segment is now served by an emerging IP market offering mixed-signal IP as well as disruptive architectures. This market is also driving innovation in process technology and 3-D packaging. With increased pixel densities, managing power has become essential. This session provides opportunity to learn about CIS IP architectures, the need for advanced sensor process technology, packaging requirements and leading applications.

18.1 IP for Disruptive Image Sensors Applications and Technologies
Jean-Luc Jaffard - *Prophesee, Paris, France*

18.2 3D Imaging for Consumer, Industrial and Automotive Applications
Korina Fotopoulou - *ams AG, Plano, TX*

18.3 Building an IP Bridge Between Image Sensor Design and Applications
Barmak Mansoorian - *Forza Silicon Corp., Pasadena, CA*

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IEEE CEDA DISTINGUISHED SPEAKER LUNCHEON: ENERGY EFFICIENT NEUROMORPHIC LEARNING AND INFERENCE AT NANOSCALE

Date: Tuesday, June 26 || Time: 12:00 - 1:30pm || Room: 3003
Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

ORGANIZER:

Gi-Joon Nam - *IEEE CEDA & IBM Research, La Jolla, CA*

Learning and adaptation are key to natural and artificial intelligence in complex and variable environments. Neural computation and communication in the brain are partitioned into the grey matter of dense local synaptic connectivity in tightly knit neuronal networks, and the white matter of sparse long-range connectivity over axonal fiber bundles across distant brain regions. This exquisite distributed multiscale organization provides inspiration to the design of scalable neuromorphic systems for deep learning and inference, with hierarchical address event-routing of neural spike events and multiscale synaptic connectivity and plasticity, and their efficient implementation in silicon low-power mixed-signal very-large-scale-integrated circuits. Advances in machine learning and system-on-chip integration have led to the development of massively parallel silicon learning machines with pervasive real-time adaptive intelligence at nanoscale that begin to approach the efficacy and resilience of biological neural systems, and already exceed the nominal energy efficiency of synaptic transmission in the mammalian brain. I will highlight examples of neuromorphic learning systems-on-chips with applications in template-based pattern recognition, vision processing, and human-computer interfaces, and outline emerging scientific directions and engineering challenges in their large-scale deployment.

Biography: Gert Cauwenberghs is Professor of Bioengineering and Co-Director of the Institute for Neural Computation at UC San Diego. He received the Ph.D. in Electrical Engineering from Caltech in 1994, and was previously Professor of Electrical and Computer Engineering at Johns Hopkins University, and Visiting Professor of Brain and Cognitive Science at MIT. His research focuses on neuromorphic engineering, adaptive intelligent systems, neuron-silicon and brain-machine interfaces, and micropower biomedical instrumentation. He is a Fellow of the Institute of Electrical and Electronic Engineers (IEEE) and the American Institute for Medical and Biological Engineering (AIMBE), and was a Francqui Fellow of the Belgian American Educational Foundation. He previously received NSF CAREER, ONR Young Investigator Program and White House PECASE awards. He served IEEE in a variety of roles including recently as Editor-in-Chief of the IEEE Transactions on Biomedical Circuits and Systems.

SPEAKER:

Gert Cauwenberghs - *Univ. of California, San Diego, La Jolla, CA*

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CEDA
IEEE Council on Electronic Design Automation

DARPA IS BUILDING A SILICON COMPILER

Time: 1:00 - 1:25 || Room: DAC Pavilion - Booth 2161 || Keywords: Emerging Architectures & Technologies. Architecture & System Design || Topic Area: EDA, Machine Learning/AI

SPEAKER:

Andreas Olofsson - *Defense Advanced Research Projects Agency, Arlington, VA*

The complexity of chips has rapidly increased in line with the predictions of Moore's law. Recent years have seen an explosion in the cost and time require to design advanced System-on-Chips (SoCs), systems-in-packages (SiPs), and PCBs. DARPA is addressing these challenges through two new electronic design automation (EDA) research programs: the Intelligent Design of Electronic Assets (IDEA) program and the Posh Open Source Hardware (POSH) program. These programs seek to form the foundation of an intelligent hardware compiler. The aim of these research efforts is to create a universal hardware compiler capable of automatically generating production ready GDSII drawings directly from source code and schematics – essentially developing the equivalent of a software compiler. Achieving this ambitious goal will require advancing the state of the art in machine learning, optimization algorithms, and expert systems. This session will discuss technical challenges associated with building a universal hardware compiler and provide analysis of the potential impact it could have on the current semiconductor ecosystem.

19

WATCH YOUR BITS: PRECISION AND FAULT TOLERANCE IN DEEP LEARNING

Time: 1:30 - 3:00pm || Room: 3014 || Event Type: Research Reviewed
Keywords: Architecture & System Design, Low-Power & Reliability
Topic Area: Machine Learning/AI, Design

CHAIR:

Muhammad Shafique - *Technische Univ. Wien, Vienna, Austria*

CO-CHAIR:

Ahmed Hemani - *KTH Royal Institute of Technology, Kista, Sweden*

Designers must account for the effect of error and imprecision on DNN behavior, especially since these characteristics of DNN can be leveraged to improve performance and energy. Ares presents a fault-injection framework for estimating the resilience of DNNs to permanent hardware faults. DeepN-JPEG revisits JPEG quantization in order to improve classification accuracy when using compressed images. ThUnderVolt enables voltage underscaling of DNN accelerators by tolerating timing errors. Loom presents an accelerator that exploits the variable precision required by different layers of a CNN, increasing performance by reducing precision.

19.1 Ares: A Framework for Quantifying the Resilience of Deep Neural Networks
Brandon Reagen, Udit Gupta, Lillian Pentecost - *Harvard Univ., Cambridge, MA*
Paul N. Whatmough - Arm Ltd. & Harvard Univ., Cambridge, MA
Sae Kyu Lee - *IBM T.J. Watson Research Center & Harvard Univ., Cambridge, MA*
Niamh Mulholland, Gu-Yeon Wei, David Brooks - *Harvard Univ., Cambridge, MA*

19.2 DeepN-JPEG: A Deep Neural Network Favorable JPEG-based Image Compression Framework
Zihao Liu, Tao Liu, Wujie Wen - *Florida International Univ., Miami, FL*
Lei Jiang - *Indiana Univ., Bloomington, IN*
Jie Xu - *University of Miami, Coral Gables, FL*
Yanzhi Wang - *Syracuse Univ., Syracuse, NY*
Gang Quan - *Florida International Univ., Miami, FL*

19.3 ThUnderVolt: Enabling Aggressive Voltage Underscaling and Timing Error Resilience for Energy Efficient Deep Learning Accelerators
Jeff Zhang - *New York Univ., Brooklyn, NY*
Kartheek Rangineni - *IIT Kanpur, India*
Zahra Ghodsi - *New York Univ., Brooklyn, NY*
Siddharth Garg - *New York Univ., New York, NY*

19.4 Loom: Exploiting Weight and Activation Precisions to Accelerate Convolutional Neural Networks
Sayeh Sharifymoghaddam, Alberto Delmas Lascorz, Patrick Judd, Andreas Moshovos - *Univ. of Toronto, Canada*

20 COMPUTE-IN-MEMORY MEETS 3DIC

Time: 1:30 - 3:00pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies, Analog & Mixed-signal Design
Topic Area: Design, Machine Learning/AI

CHAIR:
James Stine - *Oklahoma State Univ., Stillwater, OK*

CO-CHAIR:
Xuan "Silvia" Zhang - *Washington Univ. in St. Louis, MO*

From the first paper in the session you will learn how to use SRAM arrays to create binary neural networks; the second paper shows how floating-gate memory arrays can be used to accelerate analog-style vector-matrix multiplication for machine learning; the third paper focuses on how to reduce the impact of cross-coupling in TSV-based 3DICs using coding techniques; finally, the fourth paper in the session shows how turning a 3D stack on the side to create a "loaf-of-bread" structure (unlike the more common "pancake" structure) can be used in rad-hard space applications.

20.1 Parallelizing SRAM Arrays with Customized Bit-Cell for Binary Neural Networks
Rui Liu, Xiaochen Peng, Xiaoyu Sun - *Arizona State Univ., Tempe, AZ*
Win-San Khwa, Xin Si, Jia-Jing Chen, Jia-Fang Li, Meng-Fan Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Shimeng Yu - *Arizona State Univ., Tempe, AZ*

20.2 An Ultra-Low Energy Internally Analog, Externally Digital Vector-Matrix Multiplier Circuit Based on NOR Flash Memory Technology
Mohammad R. Mahmoodi, Dmitri Strukov - *Univ. of California, Santa Barbara, CA*

20.3 Coding Approach for Low-Power 3D Interconnects
Lennart J. Bamberg, Robert Schmidt, Alberto GarcÃa-Ortiz - *University of Bremen, Bremen, Germany*

20.4 A Novel 3D DRAM Memory Cube Architecture for Space Applications
Anthony D. Agnesina, Amanvir S. Sidana - *Georgia Institute of Technology, Atlanta, GA*
James Yamaguchi, Christian Krutzik, John Carson - *Irvine Sensors Corporation, Costa Mesa, CA*
Jean Yang-Scharlotta - *NASA's Jet Propulsion Lab, Pasadena, CA*
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

21 TIMING: CLOSURE, OPTIMIZATION, AND PATHFINDING

Time: 1:30 - 3:00pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Interconnects, Logic & High-Level Synthesis || Topic Area: EDA

CHAIR:
Debjit Sinha - *IBM Corp., Poughkeepsie, NY*

CO-CHAIR:
Pingqiang Zhou - *ShanghaiTech Univ., Shanghai, China*

Timing remains an essential challenge in digital design. To address it, the first paper brings a novel approximate path-based estimation model into a graph-based analysis framework; the second paper considers logic wave optimizations to optimally remove flip-flops while maintaining timing constraints. The third paper seeks to minimize the impact of DVFS sequence on power supply noise by optimizing the transition sequence of clock skipping and clock domain scheduling. Finally, the final paper develops an accurate wirelength distribution model which captures the physical aspects and the design-constraints of the system.

21.1 A General Graph Based Pessimism Reduction Framework for Design Optimization of Timing Closure
Fulin Peng, Changhao Yan - *Fudan Univ., Shanghai, China*
Chunyang Feng, Jianquan Zheng - *Synopsys, Inc., Shanghai, China*
Sheng-Guo Wang - *Univ. of North Carolina, Charlotte, NC*
Dian Zhou - *Fudan Univ. & Univ. of Texas at Dallas, TX*
Xuan Zeng - *Fudan Univ., Shanghai, China*

21.2 VirtualSync: Timing Optimization by Synchronizing Logic Waves with Sequential and Combinational Components as Delay Units
Li Zhang, Bing Li - *Technische Univ.München, Germany*
Masanori Hashimoto - *Osaka Univ., Suita, Japan*
Ulf Schlichtmann - *Technische Univ. München, Germany*

21.3 Noise-Aware DVFS Transition Sequence Optimization for Battery-Powered IoT Devices
Shaoheng Luo, **Cheng Zhuo** - *Zhejiang Univ., Hangzhou, China*
Houle Gan - *IEEE, Santa Clara, CA*

21.4 Accurate Processor-Level Wirelength Distribution Model for Technology Pathfinding Using a Modernized Interpretation of Rentâ€™s Rule
Divya Prasad - *Georgia Institute of Technology & Arm Ltd., Atlanta, GA*
Saurabh Sinha, Brian Cline, Steve Moore - *Arm Ltd., Austin, TX*
Azad Naeemi - *Georgia Institute of Technology, Atlanta, GA*

22 SPECIAL SESSION: DESIGNING SAFE AUTOMATED VEHICLES

Time: 1:30 - 3:00pm || Room: 3020 || Event Type: Special Session
Keywords: Architecture & System Design, Test & Verification
Topic Area: Automotive, ESS

CHAIR:
Selma Saidi - *Technische Universität Hamburg, Hamburg, Germany*

ORGANIZER:
Dirk Ziegenbein - *Bosch Research, Renningen, Germany*

While more and more progress is achieved and being reported in talks and press releases on the functional challenges on the road towards fully automated driving, there is little light on the challenge of proving that these automated driving functions are safe - a prerequisite for releasing automated driving functions to the market.

This special session intends to bring together academics and practitioners from automotive industry in order to show recent advances made in different aspects of this challenge. These include a model-based automated analysis and optimization method to achieve system safety, a method to reason about safety of machine learning enabled components, and the use of formal property specification to generate runtime safety monitors.

22.1 Semi-automatic Safety Analysis and Optimization
Peter Munk - *Robert Bosch GmbH, Renningen, Germany*
Andreas Abele - *Robert Bosch Automotive Steering GmbH, Schwäbisch Gmünd, Germany*
Arne Nordmann, Eike Thaden, Rakshith Amarnath, Markus Schweizer, Simon Burton - *Robert Bosch GmbH, Renningen, Germany*

22.2 Reasoning about Safety of Learning-enabled Components in Autonomous Cyber-physical Systems
Cumhur Erkan Tuncali, James P. Kapinski, Hisahiro Ito - *Toyota Research Institute of North America, Ann Arbor, MI*
Jyotirmoy Deshmukh - *Univ. of Southern California, Los Angeles, CA*

22.3 Runtime Monitoring for Safety of Intelligent Vehicles
Kosuke Watanabe, **Eunsuk Kang**, Chung-Wei Lin, Shinichi Shiraishi - *Toyota InfoTechnology Center, Mountain View, CA*

23 THE INTERNET OF THREATS

Time: 1:30 - 3:00pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies, Architecture & System Design
Topic Area: Security/Privacy, IoT

CHAIR:
Yousef Iskander - *Cisco Systems, Inc., San Jose, CA*

CO-CHAIR:
Jeyavijayan Rajendran - *Texas A&M Univ., Collage Station, TX*

This session concerns with security and privacy aspects of embedded devices from memory protection and hardware-based security to context-based authentication schemes in IoT networks as well as their connection to cloud edges.

23.1 Revisiting Context-Based Authentication in IoT
Markus Miettinen, Thien Duc Nguyen **- Technische Univ. Darmstadt, Germany**
N. Asokan - *Aalto Univ., Espoo, Finland*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

23.2 MAXelerator: FPGA Accelerator for Privacy Preserving Multiply-Accumulate (MAC) on Cloud Servers
Siam Umar Hussain, Bita Darvish Rouhani, Mohammad Ghasemzadeh, Farinaz Koushanfar - *Univ. of California, San Diego, La Jolla, CA*

23.3 Hypernel: A Hardware-Assisted Framework for Kernel Protection Without Nested Paging
Donghyun Kwon - *Seoul National Univ., Seoul, Republic of Korea*
Kuenwhee Oh - *KAIST, Yuseong-gu, Republic of Korea*
Junmo Park - *Seoul National Univ., Seoul, Republic of Korea*
Seungyong Yang - *KAIST, Yuseong-gu, Republic of Korea*
Yeongpil Cho - *Soongsil Univ., Seoul, Republic of Korea*
Brent Byunghoon Kang - *KAIST, Yuseong-gu, Republic of Korea*
Yunheung Paek - *Seoul National Univ., Seoul, Republic of Korea*

23.4 Reducing the Overhead of Authenticated Memory Encryption Using Delta Encoding and ECC Memory
Salessawi Ferede Yitbarek, Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

24 SPECIAL SESSION: THE ROAD TO NO-HUMAN-IN-THE-LOOP DESIGN

Time: 1:30 - 3:00pm || Room: 3024 || Event Type: Special Session
Keywords: Physical Design & DFM, Low-Power & Reliability, Logic & High-Level Synthesis || Topic Area: EDA, Design

CHAIR:
Noel Menezes - *Intel Corp., Hillsboro, OR*

ORGANIZER:
Andrew Kahng - *Univ. of California, San Diego, La Jolla, CA*

Today's IC design process faces a crisis of cost and risk. Both human cost (i.e., engineering expertise and effort) and schedule cost (i.e., design schedule) are barriers to leading-edge design. This crisis has spurred new research initiatives that seek to substantially reduce the cost of IC design, even to unprecedented "no-human-in-the-loop" and 24-hour turnaround time levels. This session covers technical aspects of RTL-to-GDSII design effort reduction at the leading edge of EDA and design practice -- today and in the future.

The first talk gives a big picture of how IC design can exploit cloud deployment and machine learning toward "no-human-in-the-loop" design. A talk from Qualcomm then highlights where design effort pain points exist today, as well as experiences with reinforcement learning and flow automation/autotuning. The session concludes with an EDA vendor perspective on opportunities and proof points for how EDA will enable design effort reductions for customers.

24.1 Reducing Time and Effort in IC Implementation: A Roadmap of Challenges and Solutions
Andrew Kahng - *Univ. of California, San Diego, La Jolla, CA*

24.2 Efficient Reinforcement Learning for Automating Human Decision-Making in SoC Design
Shankar Sadasivam, Rajeev Jain - *Qualcomm Technologies, Inc., San Diego, CA*
Zhuo Chen - *Carnegie Mellon Univ., Pittsburgh, PA*
Jinwon Lee - *Qualcomm, Inc., San Diego, CA*

24.3 Machine-learning Opportunities in Design Automation
Mayukh Bhattacharya - *Synopsys, Inc., Mountain View, CA*

DT25 DESIGNER TRACK: DESIGN CHALLENGES AND OPPORTUNITIES AT ADVANCED TECHNOLOGY NODES

Time: 1:30 - 3:00pm || Room: 2012 || Event Type: Designer Track Invited
Keywords: Physical Design & DFM, Interconnects || Topic Area: Design, EDA

CHAIR:
Srivaths Ravi - *Texas Instruments, Inc., Bangalore, India*

ORGANIZER:
Bertram Bradley - *GLOBALFOUNDRIES, Austin, TX*

Semiconductor technology continues to advance in search of further improved power, performance and area in a short period of time. Advanced technology node enables substantial increase in transistor density and fundamental improvements in energy efficiency, but there are new challenges in design process to unleash the benefits of continued scaling. In this session, experts from design and foundry companies will discuss challenges and opportunities in digital design process and how to tailor the specifics of the technology to meet the design requirements. Both traditional and new market segments, such as datacenter/networking, IoT, Mobile, AI/Machine learning, Automotive, and 5G Communications, will be reviewed.

25.1 Design Challenges and Comparison of Advanced Process Nodes and A Deep Dive Into Custom Hardware Development
Jeanne Trinko-Mechler - *GLOBALFOUNDRIES, Essex Junction, VT*

25.2 Designing Amazing Products on the Worlds Most Advanced Technology Platforms, What it Takes to win at 7nm and Beyond
Jung Yun Choi - *Samsung Semiconductor, Inc., Seoul, Republic of Korea*

25.3 Memory and Custom Digital Design Challenges in 10nm and 7nm Technology Nodes
Eric Karl - *Intel Corp., Hillsboro, OR*

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DT26 DESIGNER TRACK: HAVE VERIFICATION AND VALIDATION ENGINES BECOME A COMMODITY?

Time: 1:30 - 3:00pm || Room: 2010 || Event Type: Designer Track Panel
Keywords: Test & Verification, Emerging Architectures & Technologies
Topic Area: EDA, Design

MODERATOR:

Brian Bailey - *Semiconductor Engineering, Portland, OR*

ORGANIZERS:

Mark Olen - *Mentor, A Siemens Business, Wilsonville, OR*
Rebecca Granquist - *Mentor, A Siemens Business, Wilsonville, OR*

Some engineers argue that today's verification and validation engines (e.g., formal technology, simulation, emulation, and FPGA prototyping) have become a commodity with very little differentiation. And since the verification problem grows at a double exponential rate, existing verification methods based on these engines will not keep pace with growing design complexity. On the other hand, other engineers argue that today's verification engines form the foundation for a much bigger verification ecosystem, which in itself provides differentiation and has successfully allowed us to keep pace with growing design complexity. This panel of distinguish industry experts, which hold a diverse set of opposing opinions, will debate the commoditization of engines and its impact on the future of verification.

PANELISTS:

David Oesterreich - *Cypress Semiconductor Corp., San Jose, CA*
Mark Glasser - *NVIDIA Corp., Santa Clara, CA*
Ram Narayan - *Arm Ltd., Austin, TX*
Faris Khundakjie - *Intel Corp., Hudson, MA*

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IP27 IP TRACK: HAS THE TIME FOR EMBEDDED FPGA COME AT LAST?

Time: 1:30 - 3:00pm || Room: 2008 || Event Type: IP Track Invited
Keywords: Emerging Architectures & Technologies, Architecture & System Design, Reconfigurable Systems || Topic Area: IP, Design

CHAIR & ORGANIZER:

Ty Garibay - *Arteris, Inc., Austin, TX*

FPGA's have been around for more than 30 years now. For almost all of that time, chip designers have talked about merging the flexibility offered by FPGAs with fixed logic to create a centaur-like product: smart as a processor-based SoC, but with the flexible horsepower of an FPGA. In the past couple of years, several new players have entered the market for embedded FPGA IP, and there has been growing interest in this new type of IP from SoC designers. In this session, we will explore whether and why the time has come for eFPGA, and how some of the participants in this market are working to take advantage of the moment.

27.1 Increase Performance, Reduce die size with SpeedCore eFPGA Custom Blocks Flow
Steve Mensor - *Achronix Semiconductor Corp., San Jose, CA*

27.2 Dense, Portable, Scalable eFPGA & the Dragonfly System-on-Chip
Cheng Wang - *Flex Logix Technologies, Inc., Mountain View, CA*
John Teifel - *Sandia National Laboratories, Albuquerque, NM*

27.3 eFPGA for Neural Network based Image Recognition
Yoan Dupret - *Menta, Sophia-Antipolis, France*

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28 STAY COOL WITH CROSS-LAYER OPTIMIZATION!

Time: 3:30 - 5:30pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Low-Power & Reliability || Topic Area: EDA

CHAIR:
Ajay Joshi - *Boston Univ., Boston, MA*

CO-CHAIR:
Kapil Dev - *NVIDIA Corp., Santa Clara, CA*

This session addresses various energy efficient, and yet robust, schemes from application level to circuit level. The first paper presents a new quantization methodology to improve energy-efficiency of DNNs. Next paper addresses the impact of temperature on the accuracy of Re-RAM-based neuromorphic computing systems. The third paper provides a novel compiler-guided clock scheduling algorithm to minimize energy without performance degradation. Next, a memory-based energy minimization method in dual-voltage near-threshold computing systems is presented. The next paper presents a workload-dependent voltage scaling method for ultra-low-power CPUs. The last paper provides an analytical approach to characterize power delivery networks for voltage-stacked manycore systems.

28.1 Compensated-DNN: Energy Efficient Low-Precision Deep Neural Networks by Compensating Quantization Errors
Shubham Jain - *Purdue Univ., West Lafayette, IN*
Swagath Venkataramani, Vijayalakshmi Srinivasan, Jungwook Choi, Pierce I. Chuang, Leland Chang - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

28.2 Thermal-Aware Optimizations of ReRAM-Based Neuromorphic Computing Systems
Majed Valad Beigi, **Gokhan Memik** - *Northwestern Univ., Evanston, IL*

28.3 Compiler-Guided Instruction-Level Clock Scheduling for Timing Speculative Processors
Yuanbo Fan, Tianyu Jia, Jie Gu, Simone Campanoni, Russ Joseph - *Northwestern Univ., Evanston, IL*

28.4 SRAM Based Opportunistic Energy Efficiency Improvement in Dual-Supply Near-Threshold Processors
Yunfei Gu - *Univ. of Virginia, Charlottesville, VA*
Dengxue Yan - *Washington Univ., Sunnyvale, CA*
Vaibhav Verma, Mircea Stan - *Univ. of Virginia, Charlottesville, VA*
Xuan Zhang - *Washington Univ., Saint Louis, MO*

28.5 Enhancing Workload-Dependent Voltage Scaling for Energy-Efficient, Ultra-Low-Power Embedded Systems
Veni Mohan, Akhilesh Iyer, John Sartori - *Univ. of Minnesota, Twin Cities, Minneapolis, MN*

28.6 Efficient and Reliable Power Delivery in Voltage-Stacked Manycore System with Hybrid Charge-Recycling Regulators
An Zou - *Washington Univ., St. Louis, MO*
Jingwen Leng - *Shanghai Jiao Tong Univ., Shanghai, China*
Xin He - *Washington Univ., St. Louis, MO*
Yazhou Zu, Vijay Janapa Reddi - *Univ. of Texas at Austin, TX*
Xuan Zhang - *Washington Univ., Saint Louis, MO*

29 OVERCOMING OBSTACLES: ROUTING FROM ABSTRACT TO DETAIL

Time: 3:30 - 5:30pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Physical Design & DFM || Topic Area: EDA

CHAIR:
Stefanus Mantik - *Cadence Design Systems, Inc., San Jose, TX*

CO-CHAIR:
Michel Laudes - *Consultant, San Francisco, CA*

This session spans routing from Steiner tree construction to double patterning. The first paper formulates the Steiner tree problem as a minimum cost flow. Our next two papers address the ICCAD open net connection problem. The next paper considers congestion, obstacles, slew, and multiple power domains during tree construction. Our final two papers conquer detailed routing using machine learning and graph algorithms.

29.1 Exact Algorithms for Delay-Bounded Steiner Arborescences
Stephan Held, **Benjamin M. Rockel** - *Univ. of Bonn, Germany*

29.2 Efficient Multi-Layer Obstacle-Avoiding Region-to-Region Rectilinear Steiner Tree Construction
Run-Yi Wang, Chia-Cheng Pai, Jun-Jie Wang, Hsiang-Ting Wen, Yu-Cheng Pai, Yao-Wen Chang, James CM Li, Jie-Hong (Roland) Jiang - *National Taiwan Univ., Taipei, Taiwan*

29.3 Obstacle-Avoiding Open-Net Connector with Precise Shortest Distance Estimation
Guan-Qi Fang, Yong Zhong, Yi-Hao Cheng, Shao-Yun Fang - *National Taiwan Univ. of Science and Technology, Taipei, Taiwan*

29.4 COSAT: Congestion, Obstacle, and Slew Aware Tree Construction for Multiple Power Domain Design
Chien-Pang Lu - *MediaTek, Inc., Hsinchu, Taiwan*
Iris Hui-Ru Jiang - *National Taiwan Univ., Taipei, Taiwan*

29.5 A Machine Learning Framework to Identify Detailed Routing Short Violations from a Placed Netlist
Aysa Fakheri Tabrizi - *Univ. of Calgary, AB, Canada*
Nima Karimpour Darav - *Microsemi Corp., Kitchener, ON, Canada*
Shuchang Xu, Logan Rakai - *Univ. of Calgary, AB, Canada*
Ismail Bustany - *Xilinx Inc., San Jose, CA*
Andrew Kennings - *Univ. of Waterloo, ON, Canada*
Laleh Behjat - *Univ. of Calgary, AB, Canada*

29.6 DSA-Friendly Detailed Routing Considering Double Patterning and DSA Template Assignments
Hai-Juan Yu, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

30 THE AUTOMOTIVE DIGITAL TWIN – VIRTUAL OR VIRTUALLY IMPOSSIBLE...

Time: 3:30pm - 4:25pm || Room: 3020 || Event Type: Research Panel
Keywords: Test & Verification, Emerging Architectures & Technologies
Topic Area: Automotive, EDA

MODERATOR:

Vishal Kapoor - *three legged stool, San Jose, CA*

ORGANIZERS:

Bryan Ramirez - *Mentor, A Siemens Business, Longmont, CO*

Rebecca Granquist - *Mentor, A Siemens Business, Wilsonville, OR*

It's estimated that 14.2 billion miles of road testing will be required as cars reach levels 4 and 5 autonomy. Hence, some engineers argue that this is impractical and that traditional ways of testing simpler electronics using physical road testing simply will not scale. Enter the Digital Twin. The Digital Twin sets out to virtually model the complete development of these complex systems such that they can be architected, designed and tested 100% digitally before any physical hardware is created. The promise is that this will shift-left development cycles, increase quality and reduce development costs. But can a Digital Twin accurately and effectively represent an entire autonomous car to eliminate the old ways of physical validation—particularly with emerging safety requirements (ISO26262), as well as the emergence of artificial intelligence as controls? This panel of experienced technical experts will debate the pros and cons of realizing the automotive Digital Twin.

PANELISTS:

Kurt Shuler - *Arteris, Inc., Campbell, CA*
Bill Taylor - *kVA, Greenville, SC*
Sanjay Pillay - *Austemper Design, Austin, TX*
Dwight Howard - *Aptiv, Troy, MI*

31 6 SHADES OF SYNTHESIS

Time: 3:30 - 5:30pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Logic & High-Level Synthesis || Topic Area: EDA

CHAIR:

R. Iris Bahar - *Brown Univ., Providence, RI*

CO-CHAIR:

Sabya Das - *Xilinx Inc., San Jose, CA*

These six papers push the envelope of exact and approximate logic synthesis: the first paper uses convolutional neural networks to optimize the design flow for specific designs; the next three papers use satisfiability tools to improve quality and efficiency, while the last two papers advance the state of the art in approximate circuit synthesis.

31.1 Developing Synthesis Flows Without Human Knowledge
Cunxi Yu - *École Polytechnique Fédérale de Lausanne, Switzerland*
Houping Xiao - *SUNY Buffalo, NY*
Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne, Switzerland*

31.2 Efficient Computation of ECO Patch Functions
Ai Quoc Dao - *National Chung Cheng Univ., Chiayi, Taiwan*
Nian-Ze Lee - *National Taiwan Univ., Taipei City, Taiwan*
Li-Cheng Chen - *National Taiwan Univ., Taipei, Taiwan*
Mark Po-Hung Lin - *National Chung Cheng Univ., Chiayi, Taiwan*
Jie-Hong Roland Jiang - *National Taiwan Univ., Taipei, Taiwan*
Alan Mishchenko, Robert Brayton - *Univ. of California, Berkeley, CA*

31.3 Canonical Computation Without Canonical Representation
Alan Mishchenko, Robert K. Brayton - *Univ. of California, Berkeley, CA*
Ana Petkovska, Mathias Soeken - - *École Polytechnique Fédérale de Lausanne, Switzerland*
Luca Amarù - *Synopsys, Inc., Sunnyvale, CA*
Antun Domic - *Synopsys, Inc., Mountain View, CA*

31.4 SAT Based Exact Synthesis Using DAG Topology Families
Winston J. Haaswijk - - *École Polytechnique Fédérale de Lausanne, Switzerland*
Alan Mishchenko - *Univ. of California, Berkeley, CA*
Mathias Soeken, Giovanni De Micheli - - *École Polytechnique Fédérale de Lausanne, Switzerland*

31.5 Efficient Batch Statistical Error Estimation for Iterative Multi-Level Approximate Logic Synthesis
Sanbao Su, Yi Wu, Weikang Qian - *Shanghai Jiao Tong Univ., Shanghai, China*

31.6 BLASYS: Approximate Logic Synthesis Using Boolean Matrix Factorization
Soheil Hashemi, Hokchhay Tann, Sherief Reda - *Brown Univ., Providence, RI*

DT33 DESIGNER TRACK: SECURE BY DESIGN: BEST PRACTICES FOR HARDWARE SECURITY

Time: 3:30 - 5:00pm || Room: 2012 || Event Type: Designer Track Invited
Keywords: Architecture & System Design || Topic Area: Security/Privacy, Design

CHAIR:
Jason Oberg - *Tortuga Logic, San Jose, CA*

ORGANIZER:
Ryan Kastner - *Univ. of California, San Diego, CA*

As security exploits continue to be uncovered and consumers demand enhanced security from their devices, hardware designers are faced with the difficult dilemma of how to best analyze and protect their chips from security vulnerabilities. This session describes the hardware security design processes that organizations use to analyze their designs, detect flaws, and debug these issues. The speakers will discuss security audit procedures, best practices, tool flows, and other ways they meet security requirements. They will speak about beneficial tools, design methodologies, and discuss opportunities for enhancing the hardware security design process.

33.1 Hardware Security for High Consequence Systems
Vivian Kammler - *Sandia National Laboratories, Albuquerque, NM*

33.2 Securing Hardware Design: Challenges and Opportunities
Jason M. Fung - *Intel Corp., Hillsboro, OR*

33.3 Designing Security into Commercial Products
Jason Moore - *Xilinx Inc., Albuquerque, NM*

DT34 DESIGNER TRACK: POWER AND PERFORMANCE

Time: 3:30 - 5:00pm || Room: 2010 || Event Type: Designer Track Reviewed
Keywords: Low-Power & Reliability, Test & Verification, Emerging Architectures & Technologies || Topic Area: EDA, Design

CHAIR:
Vikas Sachdeva - *Real Intent, Inc., Sunnyvale, CA*

Power and performance continue to be key concerns throughout the design flow, from architecture down to circuits. In this session we will explore some front-end techniques for improving power and performance, as well as seeing their application in a neural network design.

34.1 Micgelo: A Proven Flow to Reduce Clock Tree Power with Fast TAT
Jianfeng Liu - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Saurabh Kumar Shrimal - *Mentor, A Siemens Business, Noida, India*
Minyoung Mo, Dongkwan Han, Kyungtae Do, Jung Yun Choi - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Vikas Tyagi - *Mentor Graphics (India) Pvt. Ltd. & NA, Noida UP India, India*
Minsub Byun - *Mentor, A Siemens Business, Seongnam-si, Republic of Korea*
Manish Kumar - *Mentor, A Siemens Business, Noida, India*

34.2 Efficient Power Aware DFT Methodology to Handle Implementation Challenges
Aniruddha Bhasale, Jay Shah, **Aman Jain** - *Seagate Technology, LLC, Pune, India*

34.3 Differential Energy Analysis For Improved Performance/Watt In Mobile GPU
Yadong Wang, Yu Bai, Raghu Nagaraj - *Qualcomm Technologies, Inc., San Diego, CA*
Jiaze Li - *ANSYS, Inc., San Jose, CA*
Arindam Mitra - *ANSYS, Inc., Santa Clara, CA*

34.4 A Bottom-up Methodology to Evaluate Silicon Power Consumption for a Large Number of Application-specific Scenarios
Gur Samrao - *Broadcom Limited, San Jose, CA*
Vishwajith Singh - *Synopsys, Inc., Mountain View, CA*

34.5 A Special-purpose Instruction Set and Microarchitecture for Low-power, Dynamic IoT Communication
Shahzad Muzaffar, Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology & Khalifa Univ., Abu Dhabi, United Arab Emirates*

34.6 The Quest for Easy Power-aware SW Development: A Novel Approach to DSP Code Profiling for Energy/ Performance Tradeoffs
Ioannis Savvidis - *Ericsson, Stockholm, Sweden*

IP35 IP TRACK: NEW CHALLENGES FOR IP AND VIP TO SUPPORT EMERGING APPLICATION OR ALGORITHM

Time: 3:30 - 5:00pm || Room: 2008 || Event Type: IP Track Reviewed
Keywords: Reconfigurable Systems, Emerging Architectures & Technologies
Topic Area: IP, Design

CHAIR:
Eric Esteve - *IP-nest, Marseille, France*

This session address the new challenges of IP development, verification, and integration. Design IP is by nature versatile, and we will review coherent accelerator interface as well as embedded FPGA IP development and IP securing FPGA bitstream verification. The session also covers basic needs like Multi-Gigabit-Transceivers modeling as well as future architecture supporting machine vision system, or system resilience.

35.1 Learning to Share - Embedded FPGA Timing Closure
Kent Orthner - *Achronix Semiconductor Corp., Santa Clara, CA*

35.2 Accurate System-level RNM modelling in Multi-Gigabit-Transceivers
Tobias Markus - *Heidelberg Univ., Mannheim, Germany*
Markus Mueller - *EXTOLL GmbH., Mannheim, Germany*
Ulrich Bruening - *Heidelberg Univ., Mannheim, Germany*

35.3 FPGA Bitstream-to-RTL Verification: A Case Study On An IP Module For Aerospace Applications
John Hallman - *MacAulay-Brown, Inc., Roanoke, VA*
Muhammad H. Khan - *OneSpin Solutions GmbH, München, Germany*
Sergio Marchese - *OneSpin Solutions GmbH, Bristol, United Kingdom*

35.4 Myths of System Resilience
Andrew Hopkins - *Arm Ltd., Cambridge, United Kingdom*
Andrew Tune - *Arm Ltd., Sheffield, United Kingdom*

35.5 Machine Vision IP Reference System with Intel Architecture (IA) + FPGA
Soon Ee Ong - *Intel Corp., Penang, Malaysia*
Siaw Chen Lee - *Intel Corp., Gelugor, Malaysia*

35.6 ACAI: Arm Coherent Accelerator Interface
Tutu Ajayi - *Arm Ltd. & Univ. of Michigan, Ann Arbor, MI*
Balaji Venu - *Arm Ltd., Cambridge, United Kingdom*
Paul Hartke - *Xilinx Inc., San Jose, CA*

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LATE BREAKING RESULTS

Time: 3:30 - 5:30pm || Room: 3014 || Event Type: Late Breaking Results
Keywords: Late Breaking Results

81.1 Fault-Tolerant Optical NoCs: An Approach Based on Microresonators Design Space Exploration
Mahdi Nikdast - *Colorado State Univ., Fort Collins, CO*
Gabriela Nicolescu - *École Polytechnique de Montréal, QC, Canada*
Odile Liboiron-Ladouceur - *McGill Univ., Montreal, QC, Canada*

81.2 Machine Learning Guided Application Error Analysis for Efficient Cross-Layer Resilience
Xi Liang, Yi He - *Univ. of Chicago, IL*
Prasanna Balaprakash - *Argonne National Lab, Chicago, IL*
Yanjing Li - *Univ. of Chicago, IL*

81.3 Mapping Application-Specific Topology to Reconfigurable Mesh Topology
Suleyman Tosun - *Hacettepe Univ., Ankara, Turkey*
Pinar Kullu, Yilmaz Ar - *Ankara Univ., Ankara, Turkey*

81.4 A Reconfigurable Domain-Specific Architecture for Real-Time CNN Processing at the Edge
Justin A. Sanchez, Nasim Soltani, Pratik Kulkarni, Hamed Tabkhi - *Univ. of North Carolina, Charlotte, NC*

81.5 Efficient Multi-Wafer Spatial Variation Modeling via Dual Correlated Dictionary Learning
Changhai Liao, **Jun Tao**, Yangfeng Su, Dian Zhou, Xuan Zeng - *Fudan Univ., Shanghai, China*
Xin Li - *Duke Univ. & Duke Kunshan Univ., Durham, NC*

81.6 Chained Layout Verification with Co-optimization of Pattern Library and Machine Learning Model
Haoyu Yang, Shuhe Li, Bei Yu - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*
Cyrus Tabery - *ASML, San Jose, CA*
Bingqing Lin - *Shenzhen Univ., Shenzhen, China*

81.7 A Design Flow of Accelerating Hybrid Extremely Low Bit-width Neural Network in Embedded FPGA
Junsong Wang - *IBM Research - Beijing, China*
Qiuwen Lou - *Univ. of Notre Dame, South Bend, IN*
Xiaofan Zhang - *Univ. of Illinois at Urbana-Champaign, IL*
Chao Zhu, Yonghua Lin - *IBM Research - Beijing, China*
Deming Chen - *Univ. of Illinois at Urbana-Champaign, IL*

81.8 Bit-Tactical: Exploiting Ineffectual Computations in Convolutional Neural Networks: Which, Why, and How
Alberto Lascorz, Patrick Judd, Dylan Malone Stuart, Zissis Poulos, Mostafa Mahmoud, Sayeh Sharifymoghaddam, Milos Nikolic, Kevin Siu, Andreas Moshovos - *Univ. of Toronto, ON, Canada*

LATE BREAKING RESULTS (CONTINUED)

81.9 Towards a Beyond CMOS Logic at 100 mV: Magneto-electric Spin Orbit Logic
Sasikanth Manipatruni - *Intel Corp., Hillsboro, OR*
Huichu Liu - *Intel Corp., Santa Clara, CA*
Dmitri Nikonov, Chia-Ching Lin, Tanay Gosavi - *Intel Corp., Hillsboro, OR*
Bhagwati Prasad, Yen-lin Huang - *Univ. of California, Berkeley, CA*
Kaushik Vaidyanathan - *Intel Corp., Santa Clara, CA*
Daniel Morris, Tanay Karnik - *Intel Corp., Hillsboro, OR*
Ramamoorthy Ramesh - *Intel Corp., Berkeley, CA*
Ian Young - *Intel Corp., Hillsboro, OR*

81.11 Behavioral Verification and Crossing Reduction Algorithms for pNML Devices
Matthew Morrison - *Univ. of Mississippi, Oxford, MS*

81.12 VM-CFI : Control-Flow Integrity for Virtual Machine Kernel Using Intel PT
Donghyun Kwon, **Inyoung Bang**, Jiwon Seo, Sehyun Baek, Giyeol Kim, Younghan Lee, Yunheung Paek - *Seoul National Univ., Seoul, Republic of Korea*

81.13 An Energy-Efficient Monolithic 3D-IC for Bitwise Deep Neural Networ
Hantao Huang - *Nanyang Technological Univ., Singapore*
Hao Yu - *Southern Univ. of Science and Technology, Shenzhen, China*
Bon Woong Ku, Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

81.14 An Entropy Analysis based Intrusion Detection System for Controller Area Network in Vehicles
Qian Wang - *Univ. of Maryland, College Park, MD*
Zhaojun Lu - *Huazhong Univ. of Science & Technology & Univ. of Maryland, College Park, MD*
Gang Qu - *Univ. of Maryland, College Park, MD*

81.15 Fault-Tolerant Topology Generation for 3D-NoCs
Suleyman Tosun - *Hacettepe Univ., Ankara, Turkey*
Vahid Babaei Ajabshir - *Ankara Univ., Ankara, Turkey*

81.16 Energy-Aware and Fault-Tolerant Custom Topology Design Method for NoCs
Suleyman Tosun - *Hacettepe Univ., Ankara, Turkey*
Pinar Kullu - *Ankara Univ., Ankara, Turkey*

32 WILL THE ERA OF AI DRIVE EMERGING TECHNOLOGIES TO OVERTAKE CMOS?

Time: 4:30 - 5:30pm || Room: 3024 || Event Type: Research Panel
Keywords: Emerging Architectures & Technologies || Topic Area: Machine Learning/ AI, Design

MODERATOR & ORGANIZER:

An Chen - *IBM, Durham, NC*

As CMOS scaling approaches its fundamental limit, numerous emerging technologies have been explored as potential beyond-CMOS solutions. Despite this extensive effort, few novel technologies have been shown to be able to surpass CMOS for Boolean logic and von Neumann architectures. The rise of Artificial Intelligence (AI) may provide new opportunities for emerging technologies, with significantly different applications, algorithms, architectures, and device requirements. Although customized CMOS chips can perform better than general-purpose processors for AI tasks, they are still orders of magnitude poorer than biologic brains in terms of efficiency and cognitive capabilities. While some emerging devices have shown promising characteristics to mimic neuron and synapsis, there are obvious shortcoming of these devices for large scale neural networks. This panel will bring industry and academic experts to address this question: Will the era of AI provide an opportunity for emerging technologies to overtake CMOS?

PANELISTS:

Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Meng-Fan Chang - *National Tsing Hua Univ., Hsinchu City, Taiwan*
Hsien-Hsin Sean Lee - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*
Geoffrey W. Burr - *IBM Research - Almaden, San Jose, CA*

DESIGNER/IP TRACK POSTER NETWORKING RECEPTION

Time: 5:00 - 6:00pm || Room: Level 2 Exhibit Floor || Event Type: Designer and IP Track Poster || Keywords: Any || Topic Area: Design, IP

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Designer/IP Track Poster Session held Tuesday, June 26 from 5:00 to 6:00pm on Level 2 Exhibit Floor. Designer/IP Track reviewed presentations will be included in the poster session.

124.1 Implementing Design-for-Test within a Tile-based Design Methodology using Tessent® Shell and IEEE 1687
Luc Romain - *Mentor, A Siemens Business, Kanata, Canada*
Martin Keim - *Mentor, A Siemens Business, Wilsonville, OR*
Benoit Nadeau-Dostie, Jean-François Côté - *Mentor, A Siemens Business, Kanata, Canada*
Giri Podichetty - *Mentor, A Siemens Business, Wilsonville, OR*
Albert Au - *Mentor, A Siemens Business, Kanata, Canada*
Yellapragada Venkat, Banadappa Shivaray, Suresh Raman - *Xilinx India Technology Services Pvt. Ltd., Hyderabad, India*
Ashok Anbalan - *Mentor, A Siemens Business, Bangalore, India*

124.2 A Smart Layout Merging and Review Flow for Multi_core Server CPU Design
Senhua Dong - *Huada Empyrean Software Co., Ltd, Beijing, China*
Dong Liu - *Guizhou Huaxintong Semiconductor Technologies Co., Ltd, Shanghai, China*
Qiagang Zhao, Ying Li - *Guizhou Huaxintong Semiconductor Technologies Co., Ltd, Beijing, China*
Jing Lu - *Huada Empyrean Software Co., Ltd, Beijing, China*

124.3 Novel Method for Prognosis of Plausible IR Violation Prone Regions in SOC
Prateek Pendyala, **Suryansh Sahota** - *Intel Technology India Pvt. Ltd, Bangalore, India*
Heerak Bandopadhyay - *MediaTek, Inc., Bangalore, India*

124.4 A High Efficiency SPICE Accuracy Timing Closure Flow
Wei Wei - *Huawei Technologies Co., Ltd. & HiSilicon, Shenzhen, China*
Yang Zhong - *HiSilicon, Shenzhen, China*
Xiao Yong, Senhua Dong - *Huada Empyrean Software Co., Ltd, Beijing, China*

124.5 Architectural Formal Verification of a Coherency Manager
Syed Suhaib - *NVIDIA Corp., Santa Clara, CA*
Siddartha Papineni - *NVIDIA Corp., Bangalore, India*
HarGovind Singh - *Oski Technology, Inc., Gurgaon, India*
Deepa Sahchari - *Oski Technology, Inc., Delhi, India*
Prosenjit Chatterjee - *NVIDIA Corp., Santa Clara, CA*
Vigyan Singhal - *Oski Technology, Inc., San Jose, CA*

124.6 Methodology to Improve Analog Sub-system Layout Utilization
Anantha Kamath, Pavan Kumar Kulkarni - *Texas Instruments India Pvt. Ltd., Bangalore, India*

124.8 Network-on-Chip Floorplanning Automation
Greg Ford - *GLOBALFOUNDRIES, Santa Clara, CA*

124.9 A Comprehensive Approach to Clock and Reset Domain Crossing Analysis Sign-off
Sudhakar Surendran, Venkatraman Ramakrishnan - *Texas Instruments India Pvt. Ltd., Bangalore, India*
Bijitendra Mittra - *Cadence Design Systems (India) Pvt. Ltd., Bangalore, India*
Mohammed Arif - *Texas Instruments India Pvt. Ltd., Bangalore, India*

124.10 Efficient MCMM Timing ECO on Hierarchical SoC Design with Multiple Variable Voltage Domain
Yang Zhong, Wei Wei - *Huawei Technologies Co., Ltd. & HiSilicon, Shenzhen, China*
Xiao Yong, Senhua Dong - *Huada Empyrean Software Co., Ltd, Beijing, China*

124.11 End-to-end Verification with Portable Stimulus on Mixed Signal DSP & Automotive SoCs
Courtney Fricano - *Analog Devices, Inc., Norwood, MA*
Gaurav Bhatnagar - *Analog Devices, Inc., Wilmington, MA*
Leigh Brady - *Breker Verification Systems, Inc., San Jose, CA*

124.12 Spice based Big Data Analysis for Optimal Timing Signoff on IoT Design
Chein Chi Huang, Zhen Lu - *Alchip Technologies Ltd., Shanghai, China*
Xiao Yong, Senhua Dong, Jianlin Li - *Huada Empyrean Software Co., Ltd, Beijing, China*

124.13 Reset Domain Crossing Design Bugs: The New CDC
Yossi Mirsky - *Intel Corp., Jeursalem, Israel*

124.14 Six Proven Ideas from the Field for Scalable, Reproducible Design Flows
Andrea Casotto - *Altair Engineering & Runtime Design Automation, Sunnyvale, CA*

124.15 A Modular Approach for Formally Verifying Cache Implementations
Achutha Kiran Kumar V. Madhunapantula,
Bindumadhava S. Singanamalli - *Intel Corp., Bangalore, India*
Abhijith A. Bharadwaj - *Intel Technology India Pvt. Ltd, Bangalore, India*

124.16 Mixed-signal Assertion Automation for Circuit Verification
Tracey Zhou, Selcuk Talay - *Dialog Semiconductor, Santa Clara, CA*

124.17 Functional Equivalence Verification, Not Just RTL to Netlist
Yossi Mirsky - *Intel Corp., Jeursalem, Israel*

124.18 Low Power Design by Placement Optimization in 7nm
Xiaoyue Wang, Udi Nir, Muhammad Dhodhi - *Huawei Technologies Co., Ltd., Kanata, Canada*

124.19 Layout Constrain Checks for Analog and Automotive Design
Ofer Tamir - *TowerJazz, Natanya, Israel*

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DESIGNER/IP TRACK POSTER SESSION

124.20 A Novice's Experience with Formal Connectivity Check: Visibility, Capacity, Performance, Debug and Closure
Nilesh Sonara - *Broadcom Limited, San Diego, CA*
Amir M. Nilipour - *Synopsys, Inc., San Diego, CA*
Xiaolin Chen - *Synopsys, Inc., Mountain View, CA*

124.21 Pre-CTS Power Integrity and Timing Optimization in Advanced Process Nodes
Yousuff Shariff, Savita Yelamanchili - *Qualcomm Technologies, Inc., San Diego, CA*
Pritesh Johari - *Qualcomm Technologies, Inc., San Jose, CA*
Ashok Vittal - *Qualcomm Technologies, Inc., Bangalore, India*
Badri Narayanan Ravi - *Teklatech A/S, Frederiksberg, Denmark*

124.22 Load-Aware Memory DVFS in Mobile SoC
Kyoungmin Lee, Sungchul Yoon, Chang Hoon Oh - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Tae Hee Han - *Sungkyunkwan Univ., Suwon, Republic of Korea*

124.23 Well Dependent Gate Antenna Rules
Andreas Kuesel, Andreas Martin, Uwe Mueller - *Infineon Technologies, Neubiberg, Germany*

124.24 A New IP Layout Review and Evaluation Flow
Min Jie Ji - *HiSilicon, Chengdu, China*
Jing Lu, Liwen Zhuo - *Huada Empyrean Software Co., Ltd, Beijing, China*

124.25 Bridging the Gap Between RTL & Gate Level Power Estimation in DSP Core of Advance Process Node Smartphone Chip
Sandip Ghosh - *Qualcomm India Pvt. Ltd., Bangalore, India*
Vishnu Raj, Ramachandra Rao, Vinayakam Subramanian - *ANSYS, Inc., Bangalore, India*
Arindam Mitra - *ANSYS, Inc., San Jose, CA*

124.27 Challenges and Approaches of PI Signoff for Next Generation Large Scale Network Chips
Fan Yan, Zhihua Zhou - *HiSilicon, Chengdu, China*
Huatao Yu - *HiSilicon, Shenzhen, China*
Xuewei Huang - *HiSilicon, Shanghai, China*
Xin Yao - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Shanghai, China*

124.28 Rapidly Building Next Generation Web-based EDA Applications and Platforms from Legacy Tools
Arun Joseph, Sampath G. Baddam - *IBM Systems and Technology Group, Bangalore, India*
Shashidhar Reddy, Balaji Pulluru, Pradeep Joy - *IBM Systems Group, Bangalore, India*
Wolfgang Roesner - *IBM Systems Group, Austin, TX*

124.29 Reusing Test Firmware from IP to SoC
Matthew Ballance - *Mentor, A Siemens Business, Wilsonville, OR*

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120 WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm || Room: Level 2 Lobby || Event Type: Work-In-Progress
Keywords: Any

120.1 Modeling and Optimization of Magnetic Core TSV-Inductor for On-Chip DC-DC Converter
Baixin Chen - *Zhejiang Univ., Hangzhou, China*
Umamaheswara Tida - *Univ. of Notre Dame, Notre Dame, IN*
Cheng Zhuo - *Zhejiang Univ., Hangzhou, China*
Yiyu Shi - *Univ. of Notre Dame, Notre Dame, IN*

120.2 Low-Jitter Hybrid-Mode Clock Distribution Networks
Riadul Islam - *University of Michigan, Dearborn, Dearborn, MI*
Matthew R. Guthaus - *Univ. of California, Santa Cruz, CA*

120.3 A System-Level Framework for Online Power and Supply Noise Prediction in Processor Chips
Yaguang Li - *ShanghaiTech Univ., Shanghai, China*
Cheng Zhuo - *Zhejiang Univ., Hangzhou, China*
Pingqiang Zhou - *ShanghaiTech Univ., Shanghai, China*

120.4 Path Prefetching: Accelerating Index Searches for In-Memory Databases
Shuo Li - *National Univ. of Defense Technology, Changsha, China*
Nong Xiao - *Sun Yat-sen Univ., Guangzhou, China*
Guangyu Sun - *Peking Univ., Beijing, China*
Fang Liu - *National Univ. of Defense Technology, Changsha, China*

120.5 Energy-Efficient Time-Domain Vector-by-Matrix Multiplier for Neurocomputing and Beyond
Mohammad Bavandpour, Mohammad Reza Mahmoodi, Dmitri Strukov - *Univ. of California, Santa Barbara, CA*

120.6 Enabling Hardware Efficiency With Viewer's Experience: Content-Aware Low-Power Video Memory
Jonathon D. Edstrom, Yifu Gong, Brittney Humphrey, Yiwen Xu, Jinhui Wang, **Na Gong** - *North Dakota State Univ., Fargo, ND*

120.7 Lightweight and Secure Scheme to Mitigate Denial-Of-Sleep on Wake-Up Radios for IoT Devices
Maxime Montoya, Simone Bacles-Min, Anca Molnos, Jacques J. Fournier - *CEA-LETI, Grenoble, France*

120.8 Leveraging MLC STT-RAM for Energy-Efficient CNN Training
Hengyu Zhao - *Univ. of California, Santa Cruz, CA*
Jishen Zhao - *Univ. of California, San Diego, La Jolla, CA*

120.9 Searching for the Optimal Classifier With Hardware Constraints
Xiang Lin, Ronald D. Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*

120.10 Data and Visual Analytics for the Performance Verification of High-End Processors
Yehuda Naveh, **Roi Krakovski**, Neta Dafni - *IBM Research - Haifa, Israel*
Tharunachalam Pindicura, Yan Xia - *IBM Systems Group, Austin, TX*
Brian Thompto - *IBM Systems and Technology Group, Austin, TX*

120.11 An Algorithm for Walsh Spectrum Function Classification
Michael Miller - *Univ. of Victoria, BCCanada*
Mathias Soeken - *École Polytechnique Fédérale de, Lausanne, Switzerland*

120.12 REAP: A Realtime Encryption and Authentication Protocol for In-Vehicle CAN Bus Communication
Zhaojun Lu, Qian Wang, Xi Chen, Gang Qu, Yongqiang Lyu - *Univ. of Maryland, College Park, MD*
Zhenglin Liu - *Huazhong Univ. of Science & Technology, Wuhan, China*

120.13 A Fully-Connected Ising Model Embedding Method and Its Evaluation for CMOS Annealing Machines
Kotaro Terada, **Daisuke Oku**, Sho Kanamaru, Shu Tanaka - *Waseda Univ. & Japan Science and Technology Agency, Shinjuku-ku, Japan*
Masato Hayashi - *Hitachi Ltd., Kokubunji, Japan*
Masanao Yamaoka - *Hitachi Ltd., Kokubunji-shi, Japan*
Masao Yanagisawa - *Waseda Univ., Shinjuku-ku, Japan*
Nozomu Togawa - *Waseda Univ., Tokyo, Japan*

120.14 An Approximation Algorithm to the Optimal Switch Control of Reconfigurable Battery Packs
Shih-Yu Chen, **Jie-Hong (Roland) Jiang** - *National Taiwan Univ., Taipei, Taiwan*
Shou-Hung Ling, Shih-Hao Liang, Mao-Cheng Huang - *Industrial Technology Research Institute, Chutung, Taiwan*

120.15 Use 3D Integration to Hinder Reverse Engineering Both During and After Manufacturing
Peng Gu, Dylan Stow, Shuangchen Li, Prashansa Mukim, Mahmoud Namazi, Yuan Xie - *Univ. of California, Santa Barbara, CA*

120.16 Routability Analysis with Conditional Design Rules for Sub-10nm Technologies
Ilgweon Kang, Dongwon Park - *Univ. of California, San Diego, La Jolla, CA*
Changho Han - *Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea*
Chung-Kuan Cheng - *Univ. of California, San Diego, La Jolla, CA*

120.17 CIDPro: Custom Instructions for Dynamic Program Diversification to Protect Against Timing Attacks
Arnab Kumar Biswas, Thinh H. Pham, Alexander Fell, **Siew Kei Lam** - *Nanyang Technological Univ., Singapore, Singapore*

120.18 Time Domain Simulation Based on Matrix Exponential for System-Level Power Integrity With Multiple Resonant Frequencies
Xinyuan Wang, Dongwon Park, Po-Ya Hsu - *Univ. of California, San Diego, La Jolla, CA*
Pengwen Chen - *National Chung Hsing Univ., Taichung, Taiwan*
Chung-Kuan Cheng - *Univ. of California, San Diego, La Jolla, CA*

120.19 Interference-Aware Cache Replacement Policy in MPSoC
Yen-Hao Chen - *National Tsing Hua Univ., Hsinchu, Taiwan*
Allen C. Wu - *Jiangnan Univ., Wuxi, China*
TingTing Hwang - *National Tsing Hua Univ., Hsin Chu, Taiwan*

120.20 Incremental Network Approximation on Limited Precision Neural Networks
Zheyu Liu, Kaige Jia - *Tsinghua Univ., Beijing, China*
Yuying Zhu, Weiqiang Liu - *Nanjing Univ. of Aeronautics and Astronautics, Nanjing, China*
Qi Wei, **Fei Qiao**, Ping Jin, Huazhong Yang - *Tsinghua Univ., Beijing, China*

WORK-IN-PROGRESS POSTER SESSION

120.21 Advanced DFM Analytics With Machine Learning on Layout Hotspot Prediction
Jaehwan Kim - *Samsung Electronics Co., Ltd. & Samsung Semiconductor, Inc., Gyunggi-do, Republic of Korea*
Piyush Pathak - *Cadence Design Systems, Inc., San Jose, CA*
Jae-Hyun Kang - *Samsung Electronics Co., Ltd. & Samsung Semiconductor, Inc., Yongin-si, Republic of Korea*
Byungchul Shin, Namjae Kim, Seungweon Paek, Byungmoo Song, S.-D Kwon - *Samsung Electronics Co., Ltd. & Samsung Semiconductor, Inc., Gyeonggi-do, Republic of Korea*
Philippe Hurat, Frank E. Gennari, Ya-Chieh Lai - *Cadence Design Systems, Inc., San Jose, CA*

120.22 Hardware Support for Enforcing Performance Guarantees in Multicore Processors
Jordi Cardona, Carles Hernandez, Jaume Abella - *Barcelona Supercomputing Center, Barcelona, Spain*
Francisco J. Cazorla - *Barcelona Supercomputing Center and IIIA-CSIC, Barcelona, Spain*

120.23 Application-Specific Customization of MPSoC Design for Improved Security
Benjamin Tan, Morteza Biglari-Abhari, Zoran Salcic - *Univ. of Auckland, New Zealand*

120.24 Exploiting SIMD Optimization in an ARMv7 Dynamic Binary Translator
Chih-Min Lin, Sheng-Yu Fu - *National Taiwan Univ., Taipei, Taiwan*
Ding-Yong Hong - *Academia Sinica, Taipei, Taiwan*
Yu-Ping Liu - *National Taiwan Univ., Taipei, Taiwan*
Jan-Jan Wu - *Academia Sinica, Taipei, Taiwan*
Wei-Chung Hsu - *National Taiwan Univ., Taipei, Taiwan*

120.25 An Efficient Character Generation Algorithm for High-Throughput E-Beam Lithography
Shih-Ting Lin, Hong-Yan Su, Yih-Lang Li - *National Chiao Tung Univ., HsinChu, Taiwan*
Oscar Chen - *AnaGlobe Technology, Inc., Hsinchu, Taiwan*

120.26 BOSIM: Holistic Optical Switch Models for Silicon Photonic Networks
Xuanqi Chen, Zhifei Wang - *Hong Kong Univ. of Science and Technology, Hong Kong, Hong Kong*
Yi-Shing Chang - *Intel Corp., Santa Clara, CA*
Jiang Xu, Peng Yang, Zhehui Wang, Luan H.K. Duong - *Hong Kong Univ. of Science and Technology, Hong Kong, Hong Kong*

120.27 A Cyber-Physical System Approach for Human-In-The-Loop Collision Avoidance Systems
Jin Woo Ro, Partha Roop, Avinash Malik - *Univ. of Auckland, New Zealand*

120.28 Integrated Framework for Reusable Multi-Level Embedded System Verification
Alvaro Diaz, Pablo P. Sanchez, **Eugenio Villar** - *Univ. of Cantabria, Santander, Spain*

120.29 Analytical Framework for Locality Optimization in CNN
Chi-Chung Chen, **Chia-Lin Yang** - *National Taiwan Univ., Taipei City, Taiwan*
Yi-Jou Lee - *MediaTek, Inc., Hsinchu City, Taiwan*
Bo-Cheng Lai - *National Chiao Tung Univ., Hsinchu City, Taiwan*

120.30 Design and Optimization of a Class-C/D VCO for Ultra-Low-Power IoT and Cellular Applications
Ricardo M. Martins, Nuno Lourenço, Nuno Horta - *Instituto De Telecomunicacoes & Instituto Superior Tecnico, Portugal*
Jun Yin, Pui-In Mak, Rui P. Martins - *University of Macau, Macau, China*

120.31 Cryptographically Secure Multi-Tenant Provisioning of FPGAs
Arnab Bag, **Sikhar Patranabis**, Debapriya Basu Roy, Debdeep Mukhopadhyay - *IIT Kharagpur, India*

120.32 An Optimal Microarchitecture for Stencil Computation With Data Reuse and Fine-Grained Parallelism
Yuze Chi, Peipei Zhou, Jason Cong - *Univ. of California, Los Angeles, CA*

120.34 Mixed Size Crossbar Based RRAM CNN Accelerator With Overlapped Mapping Method
Zhenhua Zhu, Ming Cheng, Jilan Lin, Lixue Xia, Hanbo Sun - *Tsinghua Univ., Beijing, China*
Xiaoming Chen - *Chinese Academy of Sciences, Beijing, China*
Yu Wang, Huazhong Yang - *Tsinghua Univ., Beijing, China*

120.35 An SoC Architecture for Learning-Based Online Anomaly Detection on ARM
Hyunyoung Oh, Younghan Lee, Hyeokjun Choe, Hayoon Yi, Yeongpil Cho, Yongje Lee, Sungroh Yoon, **Yunheung Paek** - *Seoul National Univ., Seoul, Republic of Korea*

120.36 Algorithm Selection and Design Principles for Processing in Digital RRAM Arrays: A Case Study
Feng Wang, Guojie Luo, Jiaxi Zhang, Peichen Xie, Peng Huang, Runze Han, Guangyu Sun, Jinfeng Kang - *Peking Univ., Beijing, China*

120.37 GPU-Weaver: Enabling Efficient Execution Using Dynamic Resource Sharing of Multitasking GPUs
Jiho Kim - *Hongik Univ., Seoul, Republic of Korea*
Jason Jong Kyu Park - *Univ. of Michigan, Ann Arbor, MI*
Jehee Cha - *Hongik Univ., Seoul, Republic of Korea*
Yongjun Park - *Hanyang Univ., Seoul, Republic of Korea*

120.38 XCache: Energy-Efficient In-Package Cache Architecture Using 3D-Stacked Memeristive Crosspoint
Payman Behnam, Arjun Pal Chowdhury, Nupur Rauniyar, Mahdi Bojnordi - *Univ. of Utah, Salt Lake City, UT*
Naser Sedaghati - *Imagination Technologies Ltd., San Francisco, CA*

120.39 Area Efficient Approximate Floating-Point Multipliers
Hassaan Saadat, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

120.40 DSGAN: Acceleration of Generative Adversarial Networks (GAN) Based on Dynamic Scheduling of Kernel Offloading
Chuhan Min - *Univ. of Pittsburgh, NC*
Hai Li, **Yiran Chen** - *Duke Univ., Durham, NC*

120.41 Exploiting Temporal Misalignment to Increase the Interconnect Performance for 3D Integration
Lennart J. Bamberg, Amir Najafi, Alberto GarcÃa-Ortiz - *University of Bremen, Bremen, Germany*

WORK-IN-PROGRESS POSTER SESSION

120.42 Size Optimization of MIGs With an Application to QCA and STMG Technologies
Heinz Riener, Eleonora Testa, Mathias Soeken,
Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne, Switzerland*
Luca Amarù - *Synopsys, Inc., Sunnyvale, CA*

120.43 B*-Sort: Enabling Write-Once Sorting Algorithm for Byte-Addressable Non-Volatile Memory
Yu-Pei Liang, Shuo-Han Chen, Wei-Kuan Shih,- *National Tsing Hua Univ., Hsinchu, Taiwan*
Tseng-Yi Chen, Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., Taipei, Taiwan*

NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm || Room: Level 2 Lobby || Event Type: Networking
Keywords: Any

Join us in the Level 2 Lobby to see Work-in-Progress posters and enjoy light hors d'oeuvres and beverages.

Thank You to Our Reception Sponsor

ACM SIGDA AND IEEE CEDA PH.D. FORUM

Date: Tuesday, June 26 || Time: 7:00 - 9:00pm || Room: Level 3 Lobby
Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

ORGANIZERS:

Sudeep Pasricha - *Colorado State Univ., Ft. Collins, CO*
Hai Li - *Duke Univ., Durham, NC*
Umit Ogras - *Arizona State Univ., Tempe, AZ*

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA and IEEE CEDA for senior Ph.D. students to present and discuss their dissertation research with people in the EDA community. Participation in the forum is highly competitive with acceptance rate of around 30%. The forum is open to all members of the design automation community and is free-of-charge.

For more information, please visit the ACM SIGDA Ph.D. Forum website.

Thank You to Our Sponsors

30TH ACM SIGDA UNIVERSITY DEMONSTRATION

Date: Tuesday, June 26 || Time: 7:00 - 9:00pm || Room: Level 3 Lobby
Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

ORGANIZER:

Qi Zhu - *Univ. of California, Riverside, CA*

This year marks the 30th University Demonstration at the Design Automation Conference. UD is an opportunity for university researchers to display their results and to interact with participants at DAC. Presenters and attendees at DAC are especially encouraged to participate, but participation is open to all members of the university community. The demonstrations include new EDA tools, EDA tool applications, design projects, and instructional materials.

For decades, DAC has encouraged the contributions and participation of graduate and undergraduate students globally. For further details please visit the Students & Scholarships page.

Booth Coordinators:

Chair: Qi Zhu - *Univ. of California, Riverside, CA*
Vice Chair: Anup Kumar Das - *IMEC, Peoria, IL*
Publicity Chair: Prof. Wenchao Li, - *Boston University, Boston, MA*

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VISIONARY TALK: CHALLENGES TO ENABLE 5G SYSTEM SCALING

Time: 9:00 - 9:20am || Room: 3008 || Keywords: Emerging Architectures & Technologies, Interconnects, Low Power & Reliability || Topic Areas: Design, IoT

SPEAKER:
Chidi Chidambaram - *Qualcomm, Inc., San Diego, CA*

A large fraction of the power reduction required to enable 3G and 4G came from plain digital CMOS scaling; however, at 5G, apart from the CMOS transistor, innovation from back end, other semiconductor components and their integration are required. The replacement rates for devices are slowing and the new markets for the semiconductor chips are where the chips must be built to last longer: leading us evolve from DFM, DFT to DFD – Design for Durability. Specific examples on the back-end modeling, prediction errors leading to wider product distributions and RF integration will illustrate the opportunities for the automation community in the upcoming 5G transition.

KEYNOTE: A NEW GOLDEN AGE FOR COMPUTER ARCHITECTURE: DOMAIN SPECIFIC ACCELERATORS AND OPEN RISC-V

DAVID A. PATTERSON – *Distinguished Software Engineer, Google, Inc. & Professor Emeritus, Univ. of California, Berkeley, Mountain View, CA*

Time: 9:20 - 10:00am || Room: 3008 || Keyword: Digital Design SoC & Embedded System Architectures || Topic Area: Design, Machine Learning/AI

The 1980s enjoyed architectural innovation when high-level language programming surpassed assembly language programming, which made instruction set innovation plausible, and because the Mead-Conway democratized chip design. Innovations like RISC, VLIW, and superscalar doubled performance every 18 months. The following decades saw consolidation, leveraging Moore's Law via higher clock rates and larger caches.

The ending of Moore's Law brought performance to a standstill. Processors improved only 3% last year, taking 20 years to double! Moreover, the new Spectre security enables timing attacks that leak information at ≥10 kilobits/second.

The only likely path left is changes in the instruction set architecture (ISA). For example, Domain Specific Accelerators (DSAs) can perform narrow tasks an order of magnitude more efficiently. For proprietary ISAs, we must wait years for improved chips.

The RISC-V ISA opens another path. The plasticity of FPGAs and free implementations of RISC-V enable experimental investigations of novel architectures deployed and iterated in days. FPGAs are slow but fast enough to run trillions of instructions or be deployed to test against real attacks.

Unlike proprietary ISAs, everyone can help. For tall challenges like these, we want all the best minds working on them.

We give examples of DSA chips that deliver tenfold improvements in performance-energy and sketch an example of improving RISC-V security by defeating Return Oriented Programming.

RISC-V's openness and flexibility can meet the cost-performance-energy-security demands of the Post Moore's Law era. Freeing architects from the chains of proprietary ISAs may well lead to another Golden Age for computer architecture.

Biography: After 40 years at UC Berkeley, David Patterson became an Emeritus Professor and started working in Google Brain. He is also Vice-Chair of the RISC-V Board of Directors. He has been Chair of Berkeley's CS Division, Chair of the Computing Research Association, and President of the Association for Computing Machinery. His most successful research projects have been Reduced Instruction Set Computers (RISC), Redundant Arrays of Inexpensive Disks (RAID), and Network of Workstations. This research led to many papers, seven books, and about 40 honors, including the ACM Turing Award, IEEE von Neumann Medal, member of the National Academy of Engineering, the National Academy of Sciences, the Silicon Valley Engineering Hall of Fame, and Fellow of the Computer History Museum and both AAAS societies. At Berkeley he is interested in computer architecture to improve security, and at Google he helps with future Tensor Processing Units (TPUs).

36 EMERGING STORAGE AND MEMORY TECHNOLOGIES

Time: 10:30am - 12:00pm || Room: 3014 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies || Topic Area: Design

CHAIR:
Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

CO-CHAIR:
Aviral Shrivastava - *Arizona State Univ., Tempe, AZ*

Advances in storage and memory technologies are critical for continued performance scaling of the next-generation computing systems. The first paper in this session propose an optimized NVM-based SSD with deterministic I/O latency. The second paper describes a host-managed SMR disk drive that incorporates data deduplication. The third paper presents a new wear-leveling architecture for crossbar resistive memory. Finally, the fourth paper proposes an ReRAM-based CAM (content-addressable memory) accelerator for DNA-alignment applications.

36.1 Optimized I/O Determinism for Emerging NVM-Based NVMe SSD in an Enterprise System
Seonbong Kim, Joon-Sung Yang - *Sungkyunkwan Univ., Suwon, Republic of Korea*

36.2 Improving Runtime Performance of Deduplication System With Host-Managed SMR Storage Drives
Chun-Feng Wu - *Academia Sinica and National Taiwan Univ., Taipei, Taiwan*
Ming-Chang Yang - *Chinese Univ. of Hong Kong, Hong Kong*
Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*

36.3 Wear Leveling for Crossbar Resistive Memory
Wen Wen, Youtao Zhang, Jun Yang - *Univ. of Pittsburgh, PA*

36.4 RADAR: A 3D-ReRAM Based DNA Alignment Accelerator Architecture
Wenqin Huangfu, Shuangchen Li, Xing Hu, Yuan Xie - *Univ. of California, Santa Barbara, CA*

37 MIND THE GAP IN PRODUCTIVITY AND ROBUSTNESS IN SOC DESIGN

Time: 10:30am - 12:00pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Architecture & System Design || Topic Area: EDA

CHAIR:
Andrew Putnam - *Microsoft Corporation, Redmond, WA*

CO-CHAIR:
Michael Papamichael - *Microsoft Research, Redmond, WA*

In system design we often observe a gap between modern practice and the ideal. In designs dominated by engineering cost, we look for techniques to increase productivity. The first two papers of this session aim at increasing SoC simulation and DSP-design productivity, respectively.

By contrast, the margins required to make our designs robust leave performance on the table. The remaining two papers apply thoughtful scheduling techniques to the problems of reducing the margins on Vdd required for power supply noise and the margins in timing for aging, respectively.

37.1 Mamba: Closing the Performance Gap in Productive Hardware Design Frameworks
Shunning Jiang, Berkin Ilbeyi, Christopher Batten - *Cornell Univ., Ithaca, NY*

37.2 ACED: A Hardware Library for Generating DSP Systems
Angie Wang, Paul Rigge, Adam M. Izraelevitz, Chick W. Markley, Jonathan Bachrach, Borivoje Nikolić - *Univ. of California, Berkeley, CA*

37.3 PARM: Power Supply Noise Aware Resource Management for NoC based Multicore Systems in the Dark Silicon Era
Venkata Yaswanth Raparti - *Colorado State Univ., Fort Collins, CO*
Sudeep Pasricha - *Colorado State Univ., Fort Collins, CO*

37.4 Aging-Constrained Performance Optimization for Multi Cores
Heba Khdr, Hussam Amrouch, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

38 FROM DROPLETS TO BITS: SECURITY FOR THE PHYSICAL WORLD

Time: 10:30am - 12:00pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies || Topic Area: Security/Privacy

CHAIR:
Fatemeh Tehranipoor - *San Francisco State Univ., San Francisco, CA*

CO-CHAIR:
Leyla Nazhandali - *Virtual Computing Lab, Blacksburg, VA*

The physical world presents many challenges when building secure systems, but also provides many opportunities that one can leverage for security. This session presents ideas that incorporate security and the physical world -- using manufacturing randomness to identify image sensors and security enclosures, attacking Rowhammer-based PUFs, and making microfluidic chips tamper-evident.

38.1 A Measurement System for Capacitive PUF-Based Security Enclosures
Johannes Obermaier, Vincent Immler, Matthias Hiller - *Fraunhofer Institute AISEC, Garching b. München, Germany*
Georg Sigl - *Technical University of Munich & Fraunhofer Institute AISEC,Garching b. München, Germany*

38.2 It's Hammer Time: How to Attack (Rowhammer-Based) DRAM-PUFs
Shaza Zeitouni, David Gens, Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

38.3 CamPUF: Physically Unclonable Function Based on CMOS Image Sensor Fixed Pattern Noise
Younghyun Kim, Yongwoo Lee - *Univ. of Wisconsin, Madison, WI*

38.4 Tamper-Resistant Pin-Constrained Digital Microfluidic Biochips
Jack Tang - *New York Univ., Brooklyn, NY*
Mohamed S. Ibrahim, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Ramesh Karri - *New York Univ., Brooklyn, NY*

39 SPECIAL SESSION: VERIFICATION AND VALIDATION CHALLENGES FOR DEEP NEURAL NETWORKS

Time: 10:30am - 12:00pm || Room: 3020 || Event Type: Special Session
Keywords: Test & Verification, Emerging Architectures & Technologies
Topic Area: Machine Learning/AI, Security/Privacy

CHAIR & ORGANIZER:
Siddharth Garg - *New York Univ., New York, NY*

Driven by the success of deep learning algorithms in domains ranging from image and speech recognition to autonomous driving, artificial intelligence (AI) technologies are poised to significantly impact our everyday lives. As deep learning systems gain widespread deployment, there is a critical need for verification and validation techniques that can guarantee their safety and security. In many respects, these challenges mirror those faced by both the hardware design and software systems communities; yet, the scale and computational patterns of deep neural networks (DNNs) introduce new challenges from a verification and validation standpoints. This session features talks by leading experts in the emerging domain of DNN verification (that is testing and verifying the properties of DNNs).

The first talk discusses new approaches for verifying properties of DNNs. The second presents new formal methods for the specification, verification and synthesis of deep learning systems. The third talk draws on lessons from software testing to develop new approaches for design time validation DNN properties.

39.1 Verification of Deep Neural Networks with SMT
Clark Barrett - *Stanford Univ., Stanford, CA*

39.2 Formal Methods for Deep Learning
Sanjit Seshia - *Univ. of California, Berkeley, CA*

39.3 Automated Systematic Testing of Deep Learning Systems
Suman Jana - *Columbia Univ., New York City, NY*

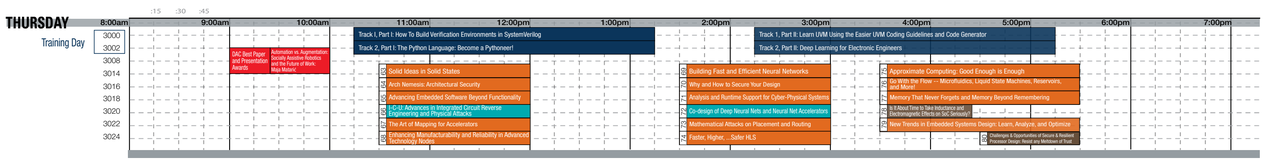
DESIGN AUTOMATION CONFERENCE

From Chips to Systems – Learn today, Create tomorrow

THURSDAY

JUNE 24-28, 2018 | SAN FRANCISCO, CA | MOSCONE CENTER WEST

Event Schedule



EVENT TYPES LEGEND

Keynotes	SKY Talks	Reviewed Presentations	Designer/IP Track Invited Presentations	Research Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

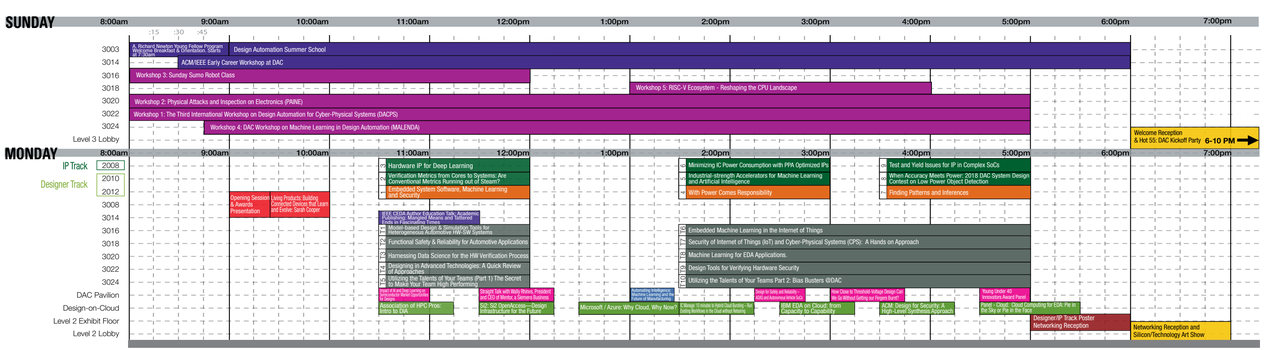
DESIGN AUTOMATION CONFERENCE

From Chips to Systems – Learn today, Create tomorrow

SUNDAY/MONDAY

JUNE 24-28, 2018 | SAN FRANCISCO, CA | MOSCONE CENTER WEST

Event Schedule



WELCOME RECEPTION & HOT 55: DAC KICK-OFF PARTY
Sunday, June 24 | 6:00 - 10:00pm | Level 3 Lobby

NETWORKING RECEPTION & SILICON/TECHNOLOGY ART SHOW
Monday, June 25 | 6:00 - 7:00pm | Level 2 Lobby

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AMIQ

EVENT TYPES LEGEND

Keynotes	SKY Talks	Reviewed Presentations	Designer/IP Track Invited Presentations	Research Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

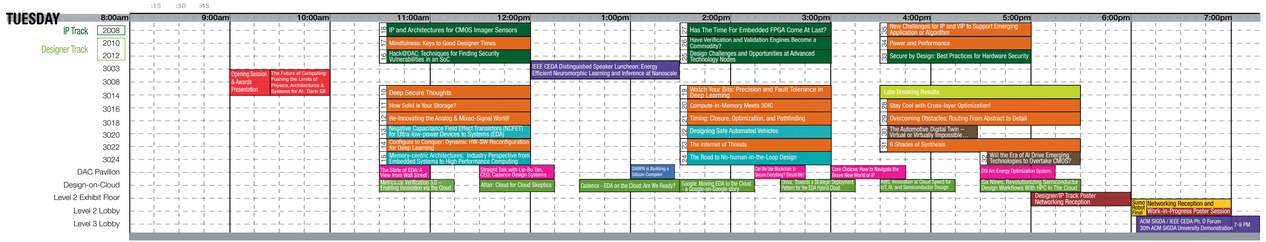
DESIGN AUTOMATION CONFERENCE

From Chips to Systems – Learn today, Create tomorrow

TUESDAY

JUNE 24-28, 2018 | SAN FRANCISCO, CA | MOSCONE CENTER WEST

Event Schedule



NETWORKING RECEPTION & WORK-IN-PROGRESS POSTER SESSION

Tuesday, June 26 | 6:00 - 7:00pm | Level 2 Lobby

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AMIQ

SUMO ROBOT FINAL COMPETITION

Tuesday, June 26 | 6:00pm | Level 2 Lobby

EVENT TYPES LEGEND

Keynotes	SKY Talks	Reviewed Presentations	Designer/IP Track Invited Presentations	Research Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

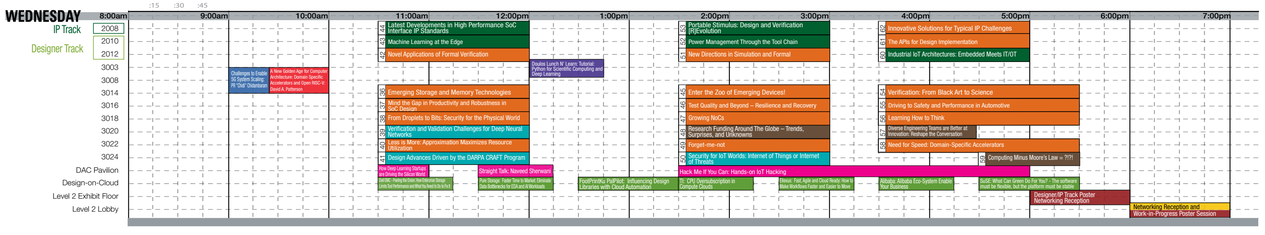
DESIGN AUTOMATION CONFERENCE

From Chips to Systems – Learn today, Create tomorrow

WEDNESDAY

JUNE 24-28, 2018 | SAN FRANCISCO, CA | MOSCONE CENTER WEST

Event Schedule



NETWORKING RECEPTION & WORK-IN-PROGRESS POSTER SESSION

Wednesday, June 27 | 6:00 - 7:00pm | Level 2 Lobby

EVENT TYPES LEGEND

Keynotes	SKY Talks	Reviewed Presentations	Designer/IP Track Invited Presentations	Research Panels	DAC Pavilion	Monday Tutorials
Workshops	Thursday is Training Day	Poster Sessions	Additional Meetings	Networking	Special Sessions	Design-on-Cloud

40 LESS IS MORE: APPROXIMATION MAXIMIZES RESOURCE UTILIZATION

Time: 10:30am - 12:00pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies, Test & Verification, Any Topic Area: ESS

CHAIR:
Akash Kumar - *Technische Univ., Dresden, Germany*

CO-CHAIR:
Charles Henri-Pierre - *CEA-LIST, Grenoble, France*

This session presents latest research that explores the use of approximate algorithms in embedded computing to solve issues of constrained resources. In particular, these papers (1) propose solutions to optimize power consumption in many-core processors and their effects on quality of service; (2) explore the tradeoffs of approximate kernels in error resilient applications in heterogeneous multicores; (3) introduce a tree-based classification algorithm as an approximation to replace heavy computation; and (4) use imprecise computation to improve task schedulability.

40.1 Approximation-Aware Coordinated Power/Performance Management for Heterogeneous Multi-Cores
Anil Kanduri - *Univ. of Turku, Finland*
Antonio Miele - *Politecnico di Milano, Italy*
Amir M. Rahmani - *Univ. of California, Irvine & Vienna Univ. of Technology, CA*
Pasi Liljeberg - *Univ. of Turku, Finland*
Cristiana Bolchini - *Politecnico di Milano, Italy*
Nikil Dutt - *Univ. of California, Irvine, CA*

40.2 QoS-Aware Stochastic Power Management for Many-Cores
Anuj Pathania - *Karlsruhe Institute of Technology, Karlsruhe., Germany*
Heba Khdr - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Muhammad Shafique - *Technische Univ., Wien, Austria*
Tulika Mitra - *National Univ. of Singapore, Singapore*
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

40.3 Employing Classification-Based Algorithms for General-Purpose Approximate Computing
Geraldo Francisco De Oliveira Junior, Larissa Rozales Gonçalves, Marcelo Brandalero, Antonio Carlos Schneider Beck, **Luigi Carro** - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

40.4 Using Imprecise Computing for Improved Non-Preemptive Real-Time Scheduling
Lin Huang - *Texas A&M Univ., College Station, TX*
Youmeng Li - *Tianjin Univ., Tianjin, China*
Sachin S. Sapatnekar - *Univ. of Minnesota, Twin Cities, Minneapolis, MN*
Jiang Hu - *Texas A&M Univ., College Station, TX*

41 SPECIAL SESSION: DESIGN ADVANCES DRIVEN BY THE DARPA CRAFT PROGRAM

Time: 10:30am - 12:00pm || Room: 3024 || Event Type: Special Session
Keywords: Emerging Architectures & Technologies, Analog & Mixed-signal Design Topic Area: Design, EDA

CHAIR & ORGANIZER:
Linton Salmon - *Defense Advanced Research Projects Agency, Arlington, VA*

DARPA's new Circuit Realization At Faster Timescales (CRAFT) program has as its goals to reduce by 10X the effort required to design and verify complex SoCs in leading edge CMOS technology and to reduce by 5X the effort required to port designs to a new fabrication process. This session will describe some of the key results from the first 15 month phase of the program, including work performed by teams led by NVidia, UC-Berkeley, and UC-San Diego.

41.1 A Modular Digital VLSI Flow for High-productivity SoC Design
Brucek Khailany, Evgeni Krimer - *NVIDIA Corp., Austin, TX*
Rangharajan Venkatesan - *NVIDIA Corp., Santa Clara, CA*
Jason Clemons - *NVIDIA Corp., Austin, TX*
Joel Emer - *NVIDIA Corp. & Massachusetts Institute of Technology, Westford, MA*
Matthew Fojtik, Alicia Klinefelter - *NVIDIA Corp., Durham, NC*
Michael Pellauer - *NVIDIA Corp., Westford, MA*
Nathaniel Pinckney - *NVIDIA Corp., Austin, TX*
Yakun Sophia Shao - *NVIDIA Corp., Santa Clara, CA*
Shreesha Srinath, Christopher Torng - *Cornell Univ., Ithaca, NY*
Sam (Likun) Xi - *Harvard Univ., Cambridge, MA*
Yanqing Zhang, Brian Zimmer - *NVIDIA Corp., Santa Clara, CA*

41.2 Enabling Generator-Based Design
Elad Alon - *Univ. of California, Berkeley, CA*

41.3 BaseJump STL: SystemVerilog Needs a Standard Template Library for Hardware Design
Michael Taylor - *Univ. of Washington, Seattle, WA*

DT42 DESIGNER TRACK: NOVEL APPLICATIONS OF FORMAL VERIFICATION

Time: 10:30am - 12:00pm || Room: 2012 || Event Type: Designer Track Reviewed
Keywords: Test & Verification, Logic & High-Level Synthesis
Topic Area: EDA, Design

CHAIR:
Homayoon Akhiani - *NVIDIA Corp., Santa Clara, CA*

Formal Verification continues to be an increasingly important toolkit for a variety of design and validation tasks. In this session we will explore formal techniques related to timing, firmware, high-level synthesis, and general validation tasks.

42.1 Timing Modeling Methodology for Formal Verification Tools
Sudhakar Surendran, Venkatraman Ramakrishnan - *Texas Instruments India Pvt. Ltd., Bangalore, India*

42.2 Acceleration Method of Sequential Equivalence Check in High-level Synthesis Design Flow
Shintaro Imamura, Tadaaki Tanimoto - *Renesas Electronics Corp., Kodaira-shi, Japan*

42.3 Formally Checking Legality of Firmware Instructions and their Combinations
Wayne Yun - *Advanced Micro Devices, Inc., Markham, ON,Canada*

42.4 Fight Fire with Formal Verification
Vincent Abikhattar, Laurent Arditi, Olivier Ponsini - *Arm Ltd., Sophia-Antipolis, France*

42.5 Formal Signoff Meets Real-world Tapeout Schedules
Puneet Anand - *Qualcomm Technologies, Inc., San Diego, CA*
Jing Gao - *Qualcomm Technologies, Inc., Santa Clara, CA*
Paras Gupta, Nishant Yadav - *Oski Technology, Inc., Gurugram, India*

42.6 Convergence Techniques for C vs. RTL Equivalence Checking
Xiushan Feng, Li You, Rachna Nambiar Jain - *Samsung Austin R&D Center, Austin, TX*
Yong Liu - *Synopsys, Inc., Mountain View, CA*

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DT43 DESIGNER TRACK: MACHINE LEARNING AT THE EDGE

Time: 10:30am - 12:00pm || Room: 2010 || Event Type: Designer Track Invited
Keywords: Architecture & System Design, Emerging Architectures & Technologies
Topic Area: Machine Learning/AI, ESS

CHAIR:
Kevin Krewell - *TIRIAS Research, Campbell, CA*

ORGANIZER:
Markus Levy - *NXP Semiconductors, Austin, TX*

As machine learning spreads across all cloud service layers, IoT devices at the edge are the next battle ground for intelligent applications that leverage local sensor data in real time, with high availability and reliable privacy. In this session we will cover the challenges of collecting sensor data from multiple sources, scaling the number of edge nodes, delivering low latency data communications, extracting data features and fusing them. Modern machine learning techniques will be presented to process the acquired data with a particular focus on scaling Deep Neural Networks from very low power microcontrollers to application processors and the power of knowledge transfer between nodes.

43.1 Machine Learning Takes Speech Recognition Performance to the Next Level
Raj Pawate - *Cadence Design Systems, Inc., Plano, TX*
Sachin Ghanekar - *Cadence Design Systems, Inc., Pune, India*

43.2 Machine Learning for Embedded Image Processing
Pavel Zemcik - *Brno Univ. of Technology, Brno, Czech Republic*

43.3 Machine Learning on Application Processors (MPU's)
Mike Caraman - *NXP Semiconductors, Bucharest, Romania*

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IP44 IP TRACK: LATEST DEVELOPMENTS IN HIGH PERFORMANCE SOC INTERFACE IP STANDARDS

Time: 10:30am - 12:00pm || Room: 2008 || Event Type: IP Track Invited
Keywords: Analog & Mixed-signal Design, Architecture & System Design, Interconnects
Topic Area: IP, Design

CHAIR & ORGANIZER:
Chirag Dhruv - *Advanced Micro Devices, Inc., Santa Clara, CA*

We live in the world where there are overlapping interface IP standards, and SOC architects face challenge of making critical decision on right interface adoption. The interface IP standards constantly evolve, and there is industry push to develop new standards to address gaps. Studying latest developments in Interface IP standards is very critical to successful product definition. This session focuses on introducing an upcoming interface technology standard, and key challenges it addresses. The session also focuses on bringing in latest developments in some of the key interface standards, upcoming trends, key application areas, and IP providers. This will help architects and product managers decide on right standard adoption for their products, and educate designers on newer developments.

44.1 High Bandwidth and Low Power USR SerDes via Chord Signaling
Amin Shokrollahi - *Kandou Bus, Lausanne, Switzerland*

44.2 Will PCIe 5.0 Become Ubiquitous in Tomorrow's SOCs?
Trupti Gowda - *PLDA, San Jose, CA*

44.3 CCIX: A New Interconnect for the Post-Moore Era
Gaurav Singh - *Xilinx Inc., San Jose, CA*

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45 ENTER THE ZOO OF EMERGING DEVICES!

Time: 1:30 - 3:00pm || Room: 3014 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies || Topic Area: Design

CHAIR:
Huichu Liu - *Intel Corp., Santa Clara, CA*

CO-CHAIR:
Xueqing Li - *Tsinghua Univ., Beijing, China*

The wide variety of emerging technologies could revolutionize an array of applications, and this session explores design techniques to maximize system-level advantages from these device technologies. The first paper presents exciting experimental results that demonstrate techniques to overcome CNTFET process variations. This is followed by a framework to minimize the power consumption of optical and electrical on-chip signals through device-system co-design. Next paper discusses techniques to decrease peak switching current, and therefore improve total energy efficiency, through the use of phase change materials. The session concludes with a proposal to use Gaussian I-V transistors for ultra-low power speech processing.

45.1 TRIG: Hardware Accelerator for Inference-Based Applications and Experimental Demonstration Using Carbon Nanotube FETs
Gage Hills, Daniel Bankman - *Stanford Univ., Stanford, CA*
Bert Moons - *Katholieke Univ. Leuven, Belgium*
Lita Yang - *Stanford Univ., Stanford, CA*
Jake Hillard - *Stanford Univ., Palo Alto, CA*
Alex B. Kahng - *Harvard Univ., Cambridge, MA*
Rebecca Park - *Stanford Univ., Stanford, CA*
Marian Verhelst - *Katholieke Univ. Leuven, Belgium*
Boris Murmann - *Stanford Univ., Stanford, CA*
Max Shulaker - *Massachusetts Institute of Technology, Cambridge, MA*
H.-S. Philip Wong, Subhasish Mitra - *Stanford Univ., Stanford, CA*

45.2 OPERON: Optical-Electrical Power-Efficient Route Synthesis for On-Chip Signals
Derong Liu, Zheng Zhao, Zheng Wang, Zhoufeng Ying, Ray Chen, David Z. Pan - *Univ. of Texas at Austin, TX*

45.3 Soft-FET: Phase Transition Material Assisted Soft Switching Field Effect Transistor for Supply Voltage Droop Mitigation
Sai Subrahmanya Teja Nibhanupudi, Jaydeep Kulkarni - *Univ. of Texas at Austin, TX*

45.4 Ultralow Power Acoustic Feature-Scoring Using Gaussian I-V Transistors
Amit Trivedi, Ahish Shylendra - *Univ. of Illinois at Chicago, IL*

46 TEST QUALITY AND BEYOND - RESILIENCE AND RECOVERY

Time: 1:30 - 3:00pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Test & Verification, Low-Power & Reliability || Topic Area: EDA

CHAIR:
Hans-Joachim Wunderlich - *Univ. Stuttgart, Germany*

CO-CHAIR:
Sybille Hellebrand - *Univ. of Paderborn, Germany*

Emerging technologies and new design techniques pose new challenges for test methods but also provide new opportunities. Additionally, current test technologies continue to be stressed by the growing complexity of silicon systems. The first two papers in this session cover advances in soft-error mitigation through a latch design resilient to both single even double upsets and single event transients, and through validation using an efficient method for hardware-based fault injections. The continued increase of test data volume requires new solutions for test compression which is the topic of the third paper. In the final paper, the inherent parallelisms and tolerance to inaccuracies of hardware accelerators can be exploited to offer new alternatives for recovery from defects.

46.1 Test Cost Reduction for X-Value Elimination By Scan Slice Correlation Analysis
Hyunsu Chae, Joon-Sung Yang - *Sungkyunkwan Univ., Suwon, Republic of Korea*

46.2 Cross-Layer Fault Space Pruning for Hardware-Assisted Fault Injection
Christian Dietrich, Achim Schmider, Oskar Pusz, Guillermo Payá Vayá, Daniel Lohmann - *Leibniz Univ. Hannover, Germany*

46.3 A Machine Learning Based Hard Fault Recuperation Model for Approximate Hardware Accelerators
Farah N. Taher - *Univ. of Texas at Dallas, TX*
Joseph Callenes-Sloan - *California Polytechnic State University, San Luis Obispo, CA*
Benjamin Carrion Schafer - *Univ. of Texas at Dallas, TX*

47 GROWING NOCS

Time: 1:30 - 3:00pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Interconnects, Architecture & System Design || Topic Area: EDA

CHAIR:
Yu-Guang Chen - *Yuan Ze Univ., Taoyuan City, Taiwan*

CO-CHAIR:
Danella Zhao - *Old Dominion Univ., Norfolk, VA*

Interconnects is the backbone of modern chips in the billion-transistor era. This session is composed of four presentations exploring novel features for network-on-chip architectures, spanning, security, efficiency through learning, and features for parallel programming models. The first paper exposes unique security vulnerabilities in emerging photonic interconnects. The second paper opens doors for machine learning techniques to improve the power efficiency of NoCs. The third paper explores hardware support for synchronization primitives for improving the performance of modern multi-core processors. The last paper explores new router architectures for alleviating memory-related bottlenecks in massively parallel accelerators such as GPGPUs.

47.1 SOTERIA: Exploiting Process Variations to Enhance Hardware Security With Photonic NoC Architectures
Sai Vineel Reddy Chittamuru, Ishan Thakkar, Varun Bhat - *Colorado State Univ., Fort Collins, CO*
Sudeep Pasricha - *Colorado State Univ., Fort Collins, CO*

47.2 LEAD: Learning-Enabled Energy-Aware Dynamic Voltage/ Frequency Scaling in NoCs
Mark Clark, Avinash Kodi, Razvan Bunescu - *Ohio Univ., Athens, OH*
Ahmed Louri - *George Washington Univ., Washington D.C.*

47.3 Subutai: Distributed Synchronization Primitives in NoC Interfaces for Legacy Parallel-Applications
Rodrigo C. Cataldo - *Univ. of South Brittany & Pontifica Univ. Católica do Rio Grande do Sul, Porto Alegre, Brazil*
Ramon C. Fernandes - *Pontifica Univ. Católica do Rio Grande do Sul, Porto Alegre, Brazil*
Kevin J. Martin - *Univ. of South Brittany & Lab-STICC, Lorient, France*
Johanna Sepulveda - *Technische Univ. München, Germany*
Altamiro A. Susin - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
César Augusto M. Marcon - *Pontifica Univ. Católica do Rio Grande do Sul, Porto Alegre, Brazil*
Jean-Philippe Diguet - *Lab-STICC & Centre National de la Recherche Scientifique, Lorient, France*

47.4 Packet Pump: Overcoming Network Bottleneck in On-Chip Interconnects for GPGPUs
Xianwei Cheng - *Univ. of North Texas, Denton, TX*
Yang Zhao - *Univ. of California, Santa Barbara, CA*
Hui Zhao - *Univ. of North Texas, Denton, TX*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

48 RESEARCH FUNDING AROUND THE GLOBE - TRENDS, SURPRISES, AND UNKNOWNS

Time: 1:30 - 3:00pm || Room: 3020 || Event Type: Research Panel
Keywords: Any || Topic Area: EDA

MODERATOR:

K.- T. Tim Cheng - *Hong Kong Univ. of Science and Technology, Hong Kong*

ORGANIZER:

K.- T. Tim Cheng - *Hong Kong Univ. of Science and Technology, Hong Kong*

Research funding is a critical driver for the electronics industry – research talent moves toward fields and regions where resources are abundant. Funding sources, strategies and trends differ dramatically across different regions of the world. This international panel of experts will discuss the similarities, differences, challenges and solutions, in research funding from a regional and global perspective, and share insights to the long-term impact of their respective funding strategies.

PANELISTS:

Shaojun Wei - *Tsinghua Univ., Beijing, China*
Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne, Switzerland*
Kenneth Plaks - *Defense Advanced Research Projects Agency, Arlington, VA*
Thyaga Nandagopal - *National Science Foundation, Alexandria, VA*

49 FORGET-ME-NOT

Time: 1:30 - 3:00pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies || Topic Area: Security/Privacy

CHAIR:

Siddharth Garg - *New York Univ., Brooklyn, NY*

CO-CHAIR:

Yier Jin - *Univ. of Florida, Gainesville, FL*

This session tackles security challenges in emerging NVMs such as data-at-rest protection and defending against malicious write streams that accelerate device wear-out.

49.1 STASH: SecuriTy Architecture for Smart Hybrid Memories
Shivam Swami, Joydeep Rakshit, Kartik Mohanram - *Univ. of Pittsburgh, PA*

49.2 ACME: Advanced Counter Mode Encryption for Secure Non-Volatile Memories
Shivam Swami, Kartik Mohanram - *Univ. of Pittsburgh, PA*

49.3 CASTLE: Compression Architecture for Secure Low Latency, Low Energy, High Endurance NVMs
Poovaiah M. Palangappa, Kartik Mohanram - *Univ. of Pittsburgh, PA*

49.4 A Collaborative Defense against Wearout Attacks in Non-Volatile Processors
Patrick T. Cronin - *Univ. of Delaware, Townsend, DE*
Chengmo Yang - *Univ. of Delaware, Newark, DE*
Yongpan Liu - *Tsinghua Univ., Beijing, China*

50 SPECIAL SESSION: SECURITY FOR IOT WORLDS: INTERNET OF THINGS OR INTERNET OF THREATS

Time: 1:30 - 3:00pm || Room: 3024 || Event Type: Special Session
Keywords: Architecture & System Design, Emerging Architectures & Technologies, Test & Verification || Topic Area: Security/Privacy, IoT

CHAIR:
Dan Holcomb - *Univ. of Massachusetts, Amherst, MA*

ORGANIZERS:
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Swarup Bhunia - *Univ. of Florida, Hall Gainesville, FL*

"Connecting the unconnected" seems to be the unstoppable technological trend as we witness the emergence of the Internet of Things (IoT), from smart homes and offices to factories, water plants, and power grids. However, without seamless security mechanisms, IoT can also be "Internet of Threats." Mitigating these frequently-changing threats requires resilient security, derived not only from a single device, but from an ensemble of devices, or the system as a whole. This session brings together recent academic research and a leading industrial perspective to identify key threats, and discuss possible approaches to mitigate the Internet of Threats in emerging applications as well as supply chains such as food-supplements, pharmaceuticals, automotive IoTs, and electronics, and highlight key challenges with IoT security and privacy as well as electronics-CAD-enabled solutions for the future.

50.1 IoT in SmartAg: Technology Applied to the Agro-food Supply Chain
John P. Verboncoeur - *Michigan State Univ., East Lansing, MI*

50.2 Protecting the Supply Chain for Automotives and IoTs
Sandip Ray - *Univ. of Florida, Gainesville, FL*
Wen Chen - *NXP Semiconductors, Austin, TX*
Rosario Cammarota - *Qualcomm Research, San Diego, CA*

50.3 Reconciling Remote Attestation and Safety-Critical Operation of Simple IoT Devices
Xavier Carpent - *Univ. of California, Irvine, CA*
Karim Eldefrawy - *SRI International, Menlo Park, CA*
Norrathep Rattanavipanon - *Univ. of California, Irvine, CA*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Gene Tsudik - *Univ. of California, Irvine, CA*

DT51 DESIGNER TRACK: NEW DIRECTIONS IN SIMULATION AND FORMAL

Time: 1:30 - 3:00pm || Room: 2012 || Event Type: Designer Track Reviewed
Keywords: Test & Verification, Logic & High-Level Synthesis
Topic Area: EDA, Design

CHAIR:
Ravindra Aneja - *Synopsys, Inc., Mountain View, CA*

Simulation continues to be an important part of the design and validation process. In this session, we will explore a variety of techniques that combine simulation with formal verification, relating to high=level modeling, functional safety, and synchronization issues. We will also present other advanced simulation techniques, addressing tricky coverage closure and asynchronous design issues.

51.1 Replay Mode for Coverage Closure and Efficient Debug
Tim Blackmore, **Jeganath G. Rajamohan**, Genevieve Bartlett - *Infineon Technologies UK Ltd., Bristol, United Kingdom*

51.2 High-speed SystemC Simulation and Formal Verification Utilizing Modular Interface
Hideki Kazama, Yoshinori Hagiwara, Takehisa Hashimoto, Hidekazu Tangi - *Sony LSI Design Inc., Atsugi, Japan*

51.3 Novel Pulse Width Insensitive Design and Verification Methods
Lakshmanan Balasubramanian - *Texas Instruments India Pvt. Ltd. & IEEE, Bangalore, India*
Ruchi Shankar, Sharavathi Bhat - *Texas Instruments India Pvt. Ltd., Bengaluru, India*
Vinaykumar S. Hegde - *Robby Technologies, Inc., Palo Alto, CA*

51.4 Accelerating Functional Coverage Analysis Using Clustering Machine Learning Techniques
Eman M. El Mandouh, Ashraf Salem - *Mentor, A Siemens Business, Cairo, Egypt*
Amr G. Wassal - *Cairo Univ., Giza, Egypt*

51.5 It's Not My Fault! How to Run a Better Fault Campaign Using Formal
Doug Smith - *Mentor, A Siemens Business, San Jose, CA*
Mark Eslinger - *Mentor, A Siemens Business, Fremont, CA*

51.6 Formal & Simulation Method to Detect Unstable States in Asynchronous State Machines
Sudhakar Surendran - *Texas Instruments India Pvt. Ltd., Bangalore, India*
Bernd Schneider - *Texas Instruments, Inc., Freising, Germany*
Kiran Rajmohan - *Texas Instruments India Pvt. Ltd., Bangalore, India*
Martin Schneider, Sebastian Fritz - *Texas Instruments, Inc., Freising, Germany*

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DT52 DESIGNER TRACK: POWER MANAGEMENT THROUGH THE TOOL CHAIN

Time: 1:30 - 3:00pm || Room: 2010 || Event Type: Designer Track Invited
Keywords: Low-Power & Reliability, Logic & High-Level Synthesis, Test & Verification
Topic Area: EDA, Design

CHAIR:
Mahiro Hikita - *Socionext, Inc., Yokohama, Japan*

ORGANIZER:
Renu Mehra - *Synopsys, Inc., San Jose, CA*

Complex power management in today's SOC low-power ASIC design affects Implementation, Verification, and Signoff aspects. Historically each of these were independent tasks with little inter-dependencies and risks. With the complex low power techniques used by designers, these flows need to work together in delivering a risk free solution with faster turn-around time (TAT). This session of industry design experts will offer differing opinions on what is needed to achieve a coherent Low Power Solution, and also look into new requirements/strategies to address growing power demands at lower geometries 7nm and below.

52.1 Implementation Challenges for Modern Low Power Chip Design
YC Wong - *Broadcom Corp., Irvine, CA*

52.2 Low Power Flow/Methodology
Godwin Maben - *Synopsys, Inc., San Jose, CA*

52.3 Low Power Sign-off Verification Challenges
Vikas Gupta - *Samsung Research America, San Jose, CA*

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IP53 IP TRACK: PORTABLE STIMULUS: DESIGN AND VERIFICATION [R]EVOLUTION

Time: 1:30 - 3:00pm || Room: 2008 || Event Type: IP Track Panel
Keywords: Test & Verification || Topic Area: IP, EDA

MODERATOR:
Martin Barnasconi - *NXP Semiconductors, Eindhoven, The Netherlands*

ORGANIZER:
Barbara Benjamin - *HighPointe Communications, Portland, OR*

The Accellera Portable Test and Stimulus Standard is the next inflection point in IP verification and system-level validation productivity. Continuing the evolution of verification standards from SystemVerilog to UVM and now Portable Stimulus, verification engineers can now apply the proven techniques of constrained randomization and abstraction at the scenario level . The standard promotes the declarative specification of abstract behaviors to be associated with design and/or verification IP components in the system, allowing test writers to compose the IP-specific behaviors into an abstract specification of their verification intent for the system-under-test. Tools will then use automation to create multiple scenarios that model the critical intent while exploring the scenario space of the system-under-test. The resulting scenarios are implemented on different platforms throughout the verification flow, including virtual platforms, simulation, emulation, FPGA prototyping and post-silicon.

The panel will explore the impact that the new Portable Test and Stimulus Standard will have on both design and verification IP, and the overall verification ecosystem.

With a variety of user perspectives, including Working Group participants as well as experienced and prospective user companies, the panel will address the following questions, as well as responding to audience questions as well:

- How will Portable Stimulus impact Verification IP? Design IP?
- Should Portable Stimulus become part of the default package delivered with an IP?
- Is Portable Stimulus an opportunity to bring design engineers more into the verification process? If so, how?
- Will RTL verification engineers and embedded software developers really use the same tool?
- Will Portable Stimulus complement or replace UVM?
- Is Portable Stimulus an evolution of verification or is it a revolution?

PANELISTS:
Adnan Hamid - *Breker Verification Systems, Inc., San Jose, CA*
Sharon Rosenberg - *Cadence Design Systems, Inc., San Jose, CA*
Tom Fitzpatrick - *Mentor, A Siemens Business, Boston, MA*
Shelly Henry - *Microsoft Corporation, Sunnyvale, CA*

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54 VERIFICATION: FROM BLACK ART TO SCIENCE

Time: 3:30 - 5:30pm || Room: 3014 || Event Type: Research Reviewed
Keywords: Test & Verification || Topic Area: EDA

CHAIR:
Vigyan Singhal - *Oski Technology, Inc., San Jose, CA*

CO-CHAIR:
Prabhat Mishra - *Univ. of Florida, Gainsville, FL*

Verification is the nemesis and nightmare of every hardware design. The cooler the features in a hardware device, the harder it is to verify. There are no shortcuts here. Whether it is real number spaces, no observability, complex designs or hard to specify features, every design is a new beast. It is difficult to scale, intellectually challenging and computationally among the hardest known problems. This session presents the entire spectrum of verification challenges and solutions- security verification, post-silicon validation, microarchitecture verification, and analog verification. Come and find out from the masters of this "black art" how it is done.

54.1 Formal Security Verification of Concurrent Firmware in SoCs using Instruction-Level Abstraction for Hardware
Bo-Yuan Huang - *Princeton Univ., Princeton, NJ*
Sayak Ray - *Intel Corp., Hillsboro, OR*
Aarti Gupta - *Princeton Univ., Princeton, NJ*
Jason M. Fung - *Intel Corp., Hillsboro, OR*
Sharad Malik - *Princeton Univ., Princeton, NJ*

54.2 Application Level Hardware Tracing for Scaling Post-Silicon Debug
Debjit Pal, Abhishek Sharma - *Univ. of Illinois at Urbana-Champaign, IL*
Sandip Ray - *Univ. of Florida, Gainesville, FL*
Flavio M. de Paula - *IBM Systems Group, Austin, TX*
Shobha Vasudevan - *Univ. of Illinois at Urbana-Champaign, IL*

54.3 Specification-Driven Automated Conformance Checking for Virtual Prototype and Post-Silicon Designs
Haifeng Gu, Mingsong Chen, Tongquan Wei - *East China Normal Univ., Shanghai, China*
Li Lei - *Intel Corp., Hillsboro, OR*
Fei Xie - *Portland State Univ., Portland, OR*

54.4 Formal Micro-Architectural Analysis of On-Chip Ring Networks
Perry van Wesel, **Julien Schmaltz** - *Eindhoven Univ. of Technology, Eindhoven, The Netherlands*

54.5 HFMV: Hybridizing Formal Methods and Machine Learning for Verification of Analog and Mixed-Signal Circuits
Hanbin Hu, Qingran Zheng, Ya Wang, Peng Li - *Texas A&M Univ., College Station, TX*

54.6 Cost-Aware Patch Generation for Multi-Target Function Rectification in Engineering Change Order
He-Teng Zhang, Jie-Hong (Roland) Jiang - *National Taiwan Univ., Taipei, Taiwan*

55 DRIVING TO SAFETY AND PERFORMANCE IN AUTOMOTIVE

Time: 3:30 - 5:30pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Architecture & System Design, Emerging Architectures & Technologies
Topic Area: Automotive, Design

CHAIR:
Eunsuk Kang - *Toyota InfoTechnology Center, Mountain View, CA*

CO-CHAIR:
Qi Zhu - *Northwestern Univ., Evanston, IL*

Future autonomous cars are currently driving innovation in the design of new automotive systems, imposing stringent constraints in terms of safety, security and performance. This session covers a wide panel of hardware and software approaches ranging from platform design to system level analysis in order to improve predictability, security, adaptability and data processing capabilities in future automotive systems.

55.1 Modelling Multicore Contention on the AURIX(TM) TC27x
Enrique Diaz - *Barcelona Supercomputing Center, Barcelonoa, Spain*
Enrico Mezzetti, **Leonidas Kosmidis**, Jaume Abella - *Barcelona Supercomputing Center, Barcelona, Spain*
Francisco J. Cazorla - *Barcelona Supercomputing Center and IIIA-CSIC, Barcelona, Spain*

55.2 Cache Side-Channel Attacks and Time-Predictability in High-Performance Critical Real-Time Systems
David Trilla, Carles Hernandez, Jaume Abella - *Barcelona Supercomputing Center, Barcelona, Spain*
Francisco J. Cazorla - *Barcelona Supercomputing Center and IIIA-CSIC & Spanish National Research Council, Barcelona, Spain*

55.3 Cross-Layer Dependency Analysis with Timing Dependence Graphs
Mischa Möstl, Rolf Ernst - *Technische Univ. Braunschweig, Germany*

55.4 Brook Auto: High-Level Certification-Friendly Programming for GPU-Powered Automotive Systems
Matina Maria Trompouki - *Univ. Politècnica de Catalunya, Spain*
Leonidas Kosmidis - *Barcelona Supercomputing Center, Barcelona, Spain*

55.5 Dynamic Vehicle Software with AUTOCONT
Christine Jakobs, Peter Tröger , Matthias Werner - *Technical Univ. of Chemnitz, Germany*
Philipp Mundhenk - *Audi Electronics Venture GmbH, Gaimersheim, Germany*
Karsten Schmidt - *Audi AG, Ingolstadt, Germany*

55.6 Automated Interpretation and Reduction of In-Vehicle Network Traces at a Large Scale
Artur Mrowca, Thomas Pramsohler - *BMW AG, München, Germany*
Sebastian Steinhorst, Uwe Baumgarten - *Technische Univ. München, Germany*

56 LEARNING HOW TO THINK

Time: 3:30 - 5:30pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies || Topic Area: Design, Machine Learning/AI

CHAIR:
Wujie Wen - *Florida International Univ., Miami, FL*

CO-CHAIR:
Yang (Cindy) Yi - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

In this session, we consider how technology impacts both training and inference in various types of neuro-inspired computing models. The first paper considers a ReRAM-based accelerator suitable for both training and inference in CNNs. The next paper presents ways to mitigate accuracy loss in spiking neural networks even when data is quantized. CNNs and binary CNNs are then considered in the context of SOT-MRAM. In papers four and five, RRAM-based compute kernels are considered in the context of sparse neural networks and gradient sparsification. The session concludes with a discussion of hyperdimensional computing.

56.1 AtomLayer: A Universal ReRAM-Based CNN Accelerator with Atomic Layer Computation
Ximing Qiao, Xiong Cao, Huanrui Yang, Linghao Song, Hai Li - *Duke Univ., Durham, NC*

56.2 Towards Accurate and High-Speed Spiking Neuromorphic Systems with Data Quantization-Aware Deep Networks
Fuqiang Liu - *Clarkson Univ., Postdam, NY*
Chenchen Liu - *Clarkson Univ., Potsdam, NY*

56.3 CMP-PIM: An Energy-Efficient Comparator-Based Processing-In-Memory Neural Network Accelerator
Shaahin Angizi, Zhezhi He, Adnan Siraj Rakin, **Deliang Fan** - *Univ. of Central Florida, Orlando, FL*

56.4 SNrram: An Efficient Sparse Neural Network Computation Architecture Based on Resistive Random-Access Memory
Peiqi Wang, Yu Ji, Chi Hong, Yongqiang Lyu, Dongsheng Wang - *Tsinghua Univ., Beijing, China*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

56.5 Long Live TIME: Improving Lifetime for Training-In-Memory Engines by Structured Gradient Sparsification
Yi Cai, Yujun Lin, Lixue Xia - *Tsinghua Univ., Beijing, China*
Xiaoming Chen - *Chinese Academy of Sciences, Beijing, China*
Song Han - *Massachusetts Institute of Technology, Cambridge, MA*
Yu Wang, Huazhong Yang - *Tsinghua Univ., Beijing, China*

56.6 Hierarchical Hyperdimensional Computing for Energy Efficient Classification
Mohsen Imani - *Univ. of California, San Diego, La Jolla, CA*
Chenyu Huang - *Univ. of California, San Diego, San Diego, CA*
Deqian Kong, Simunić Rosing - *Univ. of California, San Diego, La Jolla, CA*

57 DIVERSE ENGINEERING TEAMS ARE BETTER AT INNOVATION: RESHAPE THE CONVERSATION

Time: 3:30 - 4:25pm || Room: 3020 || Event Type: Research Panel
Keywords: Any || Topic Area: Design, EDA

MODERATOR:

Laleh Behjat - *Univ. of Calgary, AB, Canada*

ORGANIZERS:

Laleh Behjat - *Univ. of Calgary, AB, Canada*
Jayita Das - *Intel Corp., Hillsboro, OR*
Patrick Haspel - *Cadence Design Systems, Inc., San Francisco, CA*

Innovation is the key to global competitiveness in the 21st century. We try to hire the best people for our teams hoping that they will be innovative, but we never discuss what is the "best". Research shows that diversity is one of the biggest factors the performance of teams. Diverse teams solve problems and create innovative products and designs more efficiently than traditional teams. However, issues such as implicit bias can hinder the recruitment and retention efforts, and building of high-performing teams.

Join us on this panel to reshape the conversation along with industry and academic leaders. We will discuss why diversity is important for their teams, research and products, and talk about the challenges and opportunities in creating and sustaining inclusive teams. Our panellists will share their experiences and challenges encountered. They will talk about success stories of how inclusive and diverse teams were able to solve some of the most challenging EDA problems.

PANELISTS:

Ian Harris - *Univ. of California, Irvine, CA*
Kaye Mason - *Google, Inc., Mountain View, CA*
Ramon Avila - *Intel Corp., Chandler, AZ*
Neeti Bhatnagar - *Cadence Design Systems, Inc., San Francisco, CA*

58 NEED FOR SPEED: DOMAIN-SPECIFIC ACCELERATORS

Time: 3:30 - 5:30pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Architecture & System Design || Topic Area: Design

CHAIR:

Azin Ebrahimi - *KTH Royal Institute of Technology, Stockholm, Sweden*

CO-CHAIR:

Gang Quan - *Florida International Univ., Miami, FL*

This session looks at new approaches to domain specific accelerators and techniques to enable them. The session will start by looking at acceleration of robotic systems, network switches, and a brain inspired computing paradigm. The second half of the session will focus on enabling technologies for integrating accelerators, improving QoS in accelerator rich SoCs, and supporting GPGPU preemption for multi-kernel acceleration.

58.1 Dadu-P: A Scalable Accelerator for Robot Motion Planning in a Dynamic Environment
Shiqi Lian - *Univ. of Chinese Academy of Sciences & Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China*
Yinhe Han, Xiaoming Chen, Ying Wang - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*
Hang Xiao - *Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China*

58.2 Data Prediction for Response Flows in Packet Processing Cache
Hayato Yamaki - *Univ. of Electro-Communications, Chofu, Japan*
Hiroaki Nishi - *Keio Univ., Yokohama, Japan*
Shinobu Miwa, Hiroki Honda - *Univ. of Electro-Communications, Chofu, Japan*

58.3 PULP-HD: Accelerating Brain-Inspired High-Dimensional Computing on a Parallel Ultra-Low Power Platform
Fabio Montagna - *Univ. of Bologna, Italy*
Abbas Rahimi - *ETH Zurich & Univ. of California, Berkeley, Switzerland*
Simone Benatti, Davide Rossi - *Univ. of Bologna, Italy & ETH Zurich, Italy*
Luca Benini - *ETH Zurich & Univ. of Bologna, Italy, Switzerland*

58.4 Active Forwarding: Eliminate IOMMU Address Translation for Accelerator-Rich Architectures
Hsueh-Chun Fu - *National Taiwan Univ., Taipei City, Taiwan*
Po-Han Wang - *Academia Sinica, Taipei City, Taiwan*
Chia-Lin Yang - *National Taiwan Univ., Taipei City, Taiwan*

58.5 SARA: Self-Aware Resource Allocation for Heterogeneous MPSoCs
Yang Song - *Univ. of California, San Diego, La Jolla, CA*
Olivier Alavoine - *Qualcomm, Inc., San Diego, CA*
Bill Lin - *Univ. of California, San Diego, La Jolla, CA*

58.6 PEP: Proactive Checkpointing for Efficient Preemption on GPUs
Chen Li - *National Univ. of Defense Technology & Univ. of Pittsburgh, Changsha, China*
Andrew Zigerelli, Jun Yang - *Univ. of Pittsburgh, PA*
Yang Guo - *National Univ. of Defense Technology, Changsha, China*

DT60 DESIGNER TRACK: INDUSTRIAL IOT ARCHITECTURES: EMBEDDED MEETS IT/OT

Time: 3:30 - 5:00pm || Room: 2012 || Event Type: Designer Track Invited
Keywords: Architecture & System Design, Any || Topic Area: IoT, ESS

CHAIR & ORGANIZER:
Robert Oshana - *NXP Semiconductors, Austin, TX*

Large amounts of data, measured in terabytes, are generated on industrial systems today. Older data strategies drove this data to be collected in the cloud for processing and trend analysis. New data strategies have this data processed and evaluated on the industrial machine itself, with outcomes then sent to the cloud or business center. A convergence of IT and OT on industrial devices, creating a mobile/remote data center, creates a network that enables the architecture to meet the needs of the customer. The session will explore a real mobile or remote data center architecture, how safety and security are implemented, and how industrial IoT data on the machine can be turned into meaningful metadata to be sent to the cloud for further value and improvement.

60.1 Securing Edges and Fogs using Hardware and Software Technologies
Srini Addepalli - *Intel Corp., Santa Clara, CA*

60.2 Industrial IoT for Transportation
Mark Kraeling - *GE Transportation, Melbourne, FL*

60.3 Embedded IoT for Commercial Building Applications
Alin Lazar - *NXP Semiconductors, Bucuresti, Romania*

DT61 DESIGNER TRACK: THE APIS FOR DESIGN IMPLEMENTATION

Time: 3:30 - 5:00pm || Room: 2010 || Event Type: Designer Track Reviewed
Keywords: Physical Design & DFM, Analog & Mixed-signal Design
Topic Area: Design, EDA

CHAIR:
Michael Kazda - *IBM Systems Group, Poughkeepsie, NY*

Automation, Predictability, and Interoperability are key to improving designer productivity and turn-around-time for design closure. This session presents multiple techniques to achieve the same during digital and analog design. It begins with automating clock mesh construction for high-performance digital designs and using parameterized design elements for analog design. This is followed by techniques to guide design closure flows with early prediction of layout and timing issues for improved convergence and performance. It concludes with custom add-ons to achieve tool interoperability for the purpose of analog design verification.

61.1 Clock Mesh Design Methodology for Mesh Structure Exploration and Timing Optimization
Sangdo Park, Hyung-Ock Kim, Kiok Kim, Minseok Kang, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

61.2 Practical Cell Based Analog Design Methodology (AnaCell)
Akira Suzuki, **Yukichi Todoroki**, Atsushi Wada, Tomoyuki Kato, Masanori Kusano, Nobuto Ono, Kazuhiro Miura - *Jedat, Inc., Tokyo, Japan*

61.3 Integrated Early Feedback Automation Within P&R Stage for Efficient Physical Design Rule Convergence.
Giriraj Kakol, Kumaresan Vallinayagam, Nitin Tiwari, Ambar Mukherji, Vishal Sharma - *Intel Technology India Pvt. Ltd, Bangalore, India*

61.4 Sensitivity-based Clock Skew Optimization for SOC Wide-range Operation
Jiyoun Kim, Wook Kim, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

61.5 Establishment of Interoperable Analog Design Flow
Shuhei Nishida, **Saburo Hojo** - *Renesas Electronics Corp., Kodaira-shi, Japan*

61.6 Automated Circuit Topology Recognition with Analog Constraint for Robust Analog Circuit Layout Design
Yongfu Li, Valerio Perez - *GLOBALFOUNDRIES, Singapore*
Punitha Selvam - *GLOBALFOUNDRIES, Santa Clara, CA*
Vikas Tripathi - *GLOBALFOUNDRIES, Singapore*
Nishant Shah - *GLOBALFOUNDRIES, Santa Clara, CA*
Zhao Chuan Lee, I-Lun Tseng - *GLOBALFOUNDRIES, Singapore*
Jiansheng Jansen Chee - *Cadence Design Systems, Inc., San Jose, CA*
Jonathan Yoong Seang Ong - *GLOBALFOUNDRIES, Singapore*

IP62 IP TRACK: INNOVATIVE SOLUTIONS FOR TYPICAL IP CHALLENGES

Time: 3:30 - 5:00pm || Room: 2008 || Event Type: IP Track Reviewed
Keywords: Test & Verification, Architecture & System Design || Topic Area: IP, Design

CHAIR:
Chirag Dhruv - *Advanced Micro Devices, Inc., Santa Clara, CA*

This session addresses some of the upcoming trends in IP development, and how complex IP design and verification challenges are being addressed. We will review how machine learning can help solve complex IP verification challenges, how Formal Verification can address some of the complex IP challenges, and how SOC Projects can reuse IP Management to enable efficient planning and management. The speakers will share their experience about the challenges and how they have resolve those, and also touch on some of the improvement opportunities.

62.1 Topology Specification Management based on IP-XACT
Ayoung Kwon, Wonkyung Lee, Yongsoo Kim, Youngsik Kim, Seonil Brian Choi - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

62.2 Overcoming RTL: The Most-adaptable Open-source RISC-V Core
Steven F. Hoover - *Redwood EDA, Shrewsbury, MA*

62.3 Putting the I in PLM: IPLM Enables a Connected Requirements-driven SoC Methodology
Michael C. Munsey - *Methodics, Inc., San Francisco, CA*

62.4 An Automated Approach for FPU Arithmetic C-RTL Formal Verification
Aditya Tandon, Aarti Gupta, Ian G. Clifford - *Arm Ltd., Cambridge, United Kingdom*

62.5 Machine Learning in Arm CPU Verification
Stan Sokorac, **Nagesh Loke** - *Arm Ltd., Austin, TX*

62.6 Towards Fault Resilient System IP Design
John Xu - *Arm Ltd., Austin, TX*

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59 COMPUTING MINUS MOORE'S LAW = ?!?!

Time: 4:30 - 5:30pm || Room: 3024 || Event Type: Research Panel
Keywords: Architecture & System Design || Topic Area: EDA

MODERATOR & ORGANIZER:
Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

With the end of Moore's Law upon us, there is much concern for the future of computing. How will EDA and designers work together to continue creating system value without the powerful benefits of silicon dimensional scaling? Will the ultimate solution be the EDA community's ability to deliver cheaper and more productive design technologies? Or will architects rescue the day with more clever and capable accelerator designs? Or will technology save us (once again) with high-impact emerging silicon and post-silicon technologies? Or, can we steal a page from software's playbook and leverage open source as a means to greater design value? Join the panel as experts vie to define the future of computing.

PANELISTS:
Kathy Wilcox - *Advanced Micro Devices, Inc., Boxborough, MA*
David Brooks - *Harvard Univ. & Facebook, Cambridge, MA*
Yuan Xie - *Univ. of California, Santa Barbara, CA*
Krste Asanovic - *Univ. of California, Berkeley & SiFive, Inc., CA*

DESIGNER/IP TRACK POSTER NETWORKING RECEPTION

Time: 5:00 - 6:00pm || Room: Level 2 Exhibit Floor || Event Type: Designer and IP Track Poster || Keywords: Any

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Designer/IP Track Poster Session held Wednesday, June 27 from 5:00 to 6:00pm on Level 2 Exhibit Floor. Designer/IP Track reviewed presentations will be included in the poster session.

125.1 Big-data Driven, Accelerated Power Distribution Network (PDN) Optimization and Sign-off
Amruthavalli Sreekantapuram, Shailendra Dhuri - *Broadcom Communications Technologies Pvt Ltd., Bangalore, India*
Joseph Fiorenza, Kenneth Kindsfater, **Jeff Echtenkamp** - *Broadcom Inc., Irvine, CA*

125.2 Post Silicon Software Debug Technique on Emulation
Debdutta Bhattacharya - *Mentor, A Siemens Business, Fremont, CA*
Rex George, Asad Khan - *Cavium, Inc., San Jose, CA*
Ayub Khan - *Mentor, A Siemens Business, Fremont, CA*

125.3 Sensor to IoT System with No Budget
Jeff Miller - *Mentor, A Siemens Business, Wilsonville, OR*
Phil Burr - *Arm Ltd., Cambridge, United Kingdom*

125.4 Standard Cell EM Sign-off in SoC
Qiuling Zeng - *HiSilicon, Shanghai, China*
Jie Cheng - *ANSYS, Inc. & HiSilicon, Shanghai, China*
James Chuang - *Synopsys, Inc., Mountain View, CA*

125.5 Methodology for Die-scale Thermal Analysis with Thermal Netlist Considering Metal Density and Routing
Jun-Ho Choy, Valeriy Sukharev - *Mentor, A Siemens Business, Fremont, CA*
Armen Kteyan - *Mentor, A Siemens Business, Yerevan, Armenia*

125.6 A Holistic Methodology for Power-Integrity/Reliability Analysis on Low-Power Design
Suryansh Sahota, Prateek Pendyala, Munish Chauhan - *Intel Technology India Pvt. Ltd, Bangalore, India*

125.7 FLEX HTREE: Solution for Obstacle Aware Symmetrical Top Level of Clock Trees
Ranganadh V. Mudumbai, Abhinay Ponna, Uday Shankar Mudigonda - *Qualcomm India Pvt. Ltd., Bangalore, India*

125.8 Improving Design Performance Comprehending Dynamic Voltage Drop Effect
Somshekhar M. Arakeri - *Infineon Technologies, Bengaluru, India*
Soenke Grimpen, **Andreas Kuesel** - *Infineon Technologies, Neubiberg, Germany*

125.9 Comprehensive Connectivity Verification
Shahid Ikram, **Joseph D'Errico**, Yasmin Farhan, Jim Ellis - *Cavium, Inc., Marlborough, MA*
Tushar Parikh - *Synopsys, Inc., Marlborough, MA*

125.10 Making Autonomous Cars Safe
Ann M. Keffer - *Cadence Design Systems, Inc., San Jose, CA*

125.11 The UVM BATTLE FIELD: The UVM Factory Vs The UVM Callbacks
Vikas Billa - *Intel Technology India Pvt. Ltd, Hyderabad, India*

125.12 Challenges in Clock and Reset Domain Crossing Verification and Scalable Solutions
Ashish Kumar Gupta - *Broadcom Corp., Bangalore, India*
Anup Kumar Gupta - *Synopsys India Pvt. Ltd., Bangalore, India*

125.13 Efficient Modeling Styles and Methodology for Faster Gate-Level Verification
Shobana Sudhakar - *Mentor, A Siemens Business, Wilsonville, OR*
Rohit Jain - *Mentor, A Siemens Business, Fremont, CA*

125.14 Dynamic Simulation Methodology for Chip-Package-Tester ESD Verification
Sunitha Venkataraman, Jau-Wen Chen, Ting Ku - *NVIDIA Corp., Santa Clara, CA*
Akhilesh Kumar, Norman Chang, Karthik Srinivasan, Ying-Shiun Li - *ANSYS, Inc., San Jose, CA*

125.15 Analog/Mixed-Signal Verification of DRAM Peripherals with Automatically-Generated SystemVerilog Models
Yinjae Lee - *SK hynix Inc., Icheong-si Gyeonggi-do, Korea, Republic of Korea*
Jiho Lee - *Seoul National Univ., Seoul, Republic of Korea*
Keesung Han - *Scientific Analog, Inc., Palo Alto, CA*
SungYoub Jung, Seuk Son, Yunju Choi, Yoontaek Lee, SeungHeon Baek, Youngjun Kim, Sigang Ryu, Yanmei Li - *Seoul National Univ., Seoul, Republic of Korea*
Hoonam Kim, Bonggil Kang - *SK hynix Inc., Icheon-si, Republic of Korea*
Kyoungseok Rha - *Scientific Analog, Inc., Palo Alto, CA*
Daeyong Shim, Yongju Kim - *SK hynix Inc., Icheon-si, Republic of Korea*
Jaeha Kim - *Seoul National Univ., Seoul, Republic of Korea*
Shinho Chu, Sangho Lee, Junhyun Chun - *SK hynix Inc., Icheon-si, Republic of Korea*

125.16 Fast and Accurate Evaluation of Dynamic-Voltage-Drop (DVD) Impact on Timing
Palkesh Jain, Mahesh Yatagiri - *Qualcomm India Pvt. Ltd., Bangalore, India*
Vinayakam Subramaniam, Vishnu Raj - *ANSYS, Inc., Bangalore, India*

125.17 Chip Aware System Power Integrity for LDO
Sourabh Vaid - *Broadcom Limited, Irvine, CA*
Chris Ortiz - *ANSYS, Inc., San Jose, CA*
Yong Li - *Broadcom Limited, Singapore*

125.18 Performance Prediction with Varied Voltage for High Performance Computing Design
Bing Li, Xiaojing Li - *ZHAOXIN Electronic Technology Co. Ltd., Beijing, China*
Weiwei Zhang, Senhua Dong - *Huada Empyrean Software Co., Ltd, Beijing, China*

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DESIGNER/IP TRACK POSTER SESSION

125.19 For a few mV more: Vmin-driven Vectorless Algorithm for PDN Improvement
Palkesh Jain, Mahesh Yatagiri, Ashwath Prabhu, Rajagopal Narayanan - *Qualcomm India Pvt. Ltd., Bangalore, India*
Mohit Jain, David Kidd, Paul Penzes - *Qualcomm Technologies, Inc., San Diego, CA*

125.20 Automatic Approach to Insert Pipeline Flops in Complex SoC
Paul Dudek - *eSilicon Corp., Allentown, PA*
Alpesh D. Kothari, Gopinath Agrahara - *Avatar Integrated Systems Inc., Bangalore, India*

125.21 A Comprehensive Dynamic ESD Simulation for CDM Failure Diagnosis
Yan Deng - *HiSilicon, Shanghai, China*
Jie Cheng - *ANSYS, Inc. & HiSilicon, Shanghai, China*

125.22 ISO26262 Compliant Soft-error Tolerant Design Methodology
Akio Hirata, Taizo Murakami, Hiromasa Fukazawa, Kazuyuki Nakanishi, Akinori Shibayama - *Panasonic Industrial Devices Systems and Technology, Nagaokakyo City, Japan*
Abhishek Chauhan, Fadi Maamari - *Synopsys, Inc., Mountain View, CA*

125.23 How to Reduce the Complexity of Formal Analysis
Jin Hou, Mark Eslinger, Ping Yeung - *Mentor, A Siemens Business, Fremont, CA*

125.24 Leverage Advanced Analytical Techniques throughout Multiple Design Stages for Handling Power Grid Integrity in Large-Scale Designs
Antonio Todesco, Khoa Nguyen - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Sooyong Kim - *ANSYS, Inc., Palo Alto, CA*

125.25 Overcoming ESD Simulation Runtime Bottleneck using Distributed Machine Processing
Abdullah Mansoor, Muhammad Ali - *Intel Corp., Hillsboro, OR*

125.26 Hybrid Clock Tree Planner
Mukesh D. Bagul, Sangharsh Mohite, Shashank B. Sreekanta - *GLOBALFOUNDRIES, Bangalore, India*

125.27 Design and Implementation of a Scalable Neuromorphic Classifier for Emotion Detection using EEG Data
Hector Andres Gonzalez Diaz, Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology & Khalifa Univ., Abu Dhabi, United Arab Emirates*
Jerald Yoo - *National Univ. of Singapore, Singapore*

125.28 Fast Incremental Timing Analysis with Changing Macro Models
Hemlata Gupta - *IBM Corp., Poughkeepsie, NY*
Alex Suess - *IBM Server and Technology Group, Poughkeepsie, NY*
Adil Bhanji - *IBM Corp., Poughkeepsie, NY*
Michel Robert - *IBM Corp., San Francisco, CA*
Edward Hughes - *IBM Corp., Wayne, PA*
Nathan Buck - *IBM Corp., Underhill, VT*
Adam Matheny - *IBM Corp., Poughkeepse, NY*
Jack DiLullo - *IBM Corp., Austin, TX*
Jennifer Basile, Kerim Kalafala, Michael Wood - *IBM Corp., Poughkeepsie, NY*

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WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm || Room: Level 2 Lobby || Event Type: Work-In-Progress
Keywords: Any

121.1 A No-Human-In-The-Loop Methodology Toward Optimal Utilization of EDA Tools and Flows
Andrew B. Kahng, Shriram C. Kumar, **Tushar Shah** - *Univ. of California, San Diego, LaJolla, CA*

121.2 A Robust Digital RRAM-based Convolutional Block for Low Energy Image Processing and Learning Applications
Edouard Giacomin - *Univ. of Utah, Salt Lake City, UT*
Tzofnat Greenberg, Shahar Kvatinsky - *Technion - Israel Institute of Technology, Haifa, Israel*
Pierre-Emmanuel Gaillardon - *Univ. of Utah, Salt Lake City, UT*

121.3 Towards Scalable Vectorless Thermal Integrity Verification
Zhiqiang Zhao - *Michigan Technological Univ., Hancock, MI*
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

121.4 Always-ON Visual Node With a Hardware-Software Event-Based Binarized Neural Network Inference Engine
Manuele Rusci, Davide Rossi - *Univ. of Bologna, Italy & ETH Zurich, Italy*
Eric Flamand - *Greenwave Systems, Villard-Bonnot, France*
Massimo Gottardi - *Fondazione Bruno Kessler, Trento, Italy*
Elisabetta Farella - *Fondazione Bruno Kessler, Povo, Italy*
Luca Benini - *ETH Zurich & Univ. of Bologna, Italy, Switzerland*

121.6 Chasing Tails: Reliability-Aware Feasibility Analysis for Analog System Design
Maike Taddiken, Theodor Hillebrand, Steffen Paul, Dagmar Peters-Drolshagen - *University of Bremen, Germany*

121.7 Don't Forget the Serial Equivalency: Parallelizing FPGA Routing Based on Dependency-Aware Scheduling
Minghua Shen - *Sun Yat-sen Univ., Guangzhou, China*
Wentai Zhang, Jxzhang Zhang - *Peking Univ., Beijing, China*
Nong Xiao - *Sun Yat-sen Univ., Guangzhou, China*
Guojie Luo - *Peking Univ., Beijing, China*

121.8 SOFIA: A Fault Injection Tool for Detailed and Efficient Multicore Soft Error Vulnerability Analysis
Felipe Rosa - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
Luciano Ost - *Loughborough Univ., Leicester, United Kingdom*
Gennaro S. Rodrigues, Fernanda Kastensmidt, Ricardo Reis - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
Simon Davidmann, Larry Lapides - *Imperas Software Ltd., Thame, United Kingdom*

121.9 Layout-Aware Embedding of Quantum-Dot Cellular Automata Networks Onto a Quantum Annealer
Jose P. Pinilla, Steven Wilton - *Univ. of British Columbia, Vancouver, Canada*

121.10 AERIS: Area/Energy-Efficient 1T2R ReRAM Based Processing-In-Memory Neural Network System-On-A-Chip
Jinshan Yue, **Yongpan Liu**, Fang Su, Zhe Yuan, Zhibo Wang, Wenyu Sun, Xueqing Li, Huazhong Yang - *Tsinghua Univ., Beijing, China*
Shuangchen Li - *Univ. of California, Santa Barbara, CA*

121.11 Low Overhead Online Checkpoint for Intermittently Powered Non-volatile FPGAs
Xinyi Zhang - *Univ. of Pittsburgh, PA*
Patterson Clay - *Oklahoma State Univ., Stillwater, OK*
Yongpan Liu - *Tsinghua Univ., Beijing, China*
Chengmo Yang - *Univ. of Delaware, Newark, DE*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
Jingtong Hu - *Univ. of Pittsburgh, PA*

121.12 TAP: Reducing the Energy of Asymmetric Hybrid Last-Level Cache via Thrashing Aware Placement and Migration
Jing-Yuan Luo, **Ing-Chao Lin** - *National Cheng Kung Univ., Tainan, Taiwan*
Hsiang-Yun Cheng - *Academia Sinica, Taipei, Taiwan*
Da-Wei Chang - *National Cheng Kung Univ., Tainan, Taiwan*

121.13 Spectral Approach to Verifying Non-Linear Arithmetic Circuits
Cunxi Yu - *École Polytechnique Fédérale de Lausanne, Switzerland*
Maciej Ciesielski - *Univ. of Massachusetts, Amherst, MA*

121.14 Log-Based Cache Design for Sequential-Write-Constrained Shingled Magnetic Recording Disks
Yong-Ching Lin, **Shuo-Han Chen** - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yuan-Hao Chang, Tseng-Yi Chen - *Academia Sinica, Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., Taipei, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

121.15 Optimizing Pipelined Heterogeneous FPGAs for Convolutional Neural Networks
Weiwen Jiang - *Univ. of Pittsburgh & Chongqing Univ., PA*
Edwin H.-M. Sha - *Chongqing Univ. & East China Normal Univ., Chongqing, China*
Qingfeng Zhuge - *East China Normal Univ., Chongqing, China*
Lei Yang - *Univ. of California, Irvine & Chongqing Univ., CA*
Xianzhang Chen - *Chongqing Univ., Chongqing, China*
Jingtong Hu - *Univ. of Pittsburgh, PA*

121.16 Accurate Emulation of a State-Of-The-Art Mobile CPU/GPU Platform
Kuba Kaszyk, Harry Wagstaff, Tom Spink, Björn Franke, Mike O'Boyle - *Univ. of Edinburgh, United Kingdom*
Henrik Uhrenholt - *Arm Ltd., Lund, Sweden*

121.17 Test Methodology for PCHB/PCFB Based Asynchronous Pipeline Circuits
Ting-Yu Shen - *National Taiwan Univ., Taipei City, Taiwan*
Chia-Cheng Pai - *National Taiwan Univ., Taipei, Taiwan*
Tsai-Chieh Chen - *National Taiwan Univ., Taipei City, Taiwan*
James C-M Li - *National Taiwan Univ., Taiwan, Taiwan*

121.18 Understanding and Benchmarking the Capabilities and Limitations of SAT Solvers in Defeating Obfuscation Schemes
Shervin Roshanisefat, Harshith Kumar Thirumala, Kris Gaj, Houman Homayoun, Avesta Sasan - *George Mason Univ., Fairfax, VA*

WORK-IN-PROGRESS POSTER SESSION

121.19 RMAC: Runtime Configurable Floating Point Multiplier for Approximate Computing
Mohsen Imani - *Univ. of California, San Diego, La Jolla, CA*
Ricardo A. Garcia - *Univ. of California, San Diego, LaJolla, CA*
Saransh Gupta, Tajana Simunić Rosing - *Univ. of California, San Diego, La Jolla, CA*

121.20 Scalable and Efficient Multi-Queue Access to FPGA-Based Multi-Accelerators
Siavash Rezaei - *Univ. of California, Irvine, United States*
Kanghee Kim - *Soongsil Univ., Seoul, Republic of Korea*
Eli Bozorgzadeh - *Univ. of California, Irvine, CA*

121.21 PARADISE - PostMoore Architecture and Accelerator Design Space Exploration Using Device Level Simulation and Experiments
Dilip Vasudevan, George Michelogiannakis, David Donofrio, John Shalf - *Lawrence Berkeley National Lab, Berkeley, CA*

121.22 IgnoreTM: Ignoring Timing Violations With Transactional Memory
Sungseob Whang - *Brown Univ., Boston, MA*
Dimitra Papagiannopoulou - *Univ. of Massachusetts, Lowell, MA*
Tali Moreshet - *Boston Univ., Boston, MA*
Iris Bahar - *Brown Univ., Providence, RI*

121.23 AILocker: Authenticated Image Locker for Video
Jihye Kim - *Kookmin Univ., Seoul, Republic of Korea*
Hankyung Ko, Hyunok Oh - *Hanyang Univ., Seoul, Republic of Korea*

121.24 Defining and Detecting Synthesis-Generated Glitches
Yan Peng, Mark Greenstreet - *Univ. of British Columbia, Vancouver, Canada*
Ian W. Jones - *Oracle Labs, Redwood Shores, CA*

121.25 On-Chip CNN Accelerator for Image Super-Resolution
Jung-Woo Chang, Suk-Ju Kang - *Sogang Univ., Seoul, Republic of Korea*

121.26 HRM: H-tree Based Reconfiguration Mechanism in Homogeneus PE Array for Video Processing
Lin Jiang, Xueting Zhang, **Junyong Deng** - *Xi'an University of Posts and Telecommunications, Xi'an, China*
Shuang Song, Lizy K. John - *Univ. of Texas at Austin, TX*

121.27 Fast and Efficient In-Memory Processing for Different Memory Technologies
Saransh Gupta, Mohsen Imani, Tajana Simunić Rosing - *Univ. of California, San Diego, La Jolla, CA*

121.29 Placement-Aware Layout Generation of One-Dimensional FinFET Standard Cells
Mei-Yen Chiu, **Jie-Hong (Roland) Jiang** - *National Taiwan Univ., Taipei, Taiwan*

121.30 BoxPlacer: Force Directed-Based Timing-Driven Placement for FPGAs
Minghua Shen - *Sun Yat-sen Univ., Guangzhou, China*
jxzhang Zhang, Wentai Zhang - *Peking Univ., Beijing, China*
Nong Xiao - *Sun Yat-sen Univ., Guangzhou, China*
Guojie Luo - *Peking Univ., Beijing, China*

121.31 Frequency Optimization of Systolic Array-Based DNNs on FPGAs
Jiaxi Zhang, Wentai Zhang, Guojie Luo, Xuechao Wei, Yun Liang - *Peking Univ., Beijing, China*
Jason Cong - *Univ. of California, Los Angeles, CA*
Minghua Shen, Nong Xiao - *Sun Yat-sen Univ., Guangzhou, China*

121.32 Edge-Host Partitioning of Deep Neural Networks With Feature Space Encoding for Resource-Constrained Internet-of-Things Platforms
Jong Hwan Ko, Taesik Na, Mohammad F. Amir, Saibal Mukhopadhyay - *Georgia Institute of Technology, Atlanta, GA*

121.33 Achieving Performance Balance for Dual-Criticality System Based on ARM TrustZone
Pan Dong - *National Univ. of Defense Technology & Univ. of York, United Kingdom*
Alan Burns, Zhe Jiang - *Univ. of York, United Kingdom*
Yan Ding, Long Gao - *National Univ. of Defense Technology, Changsha, China*

121.34 Architecture Exploration and Delay Minimization Synthesis for SET-Based Programmable Gate Arrays
Chia-Cheng Wu - *National Tsing Hua Univ., Hsinchu, Taiwan*
Kung-Han Ho, **Juinn-Dar Huang** - *National Chiao Tung Univ., Hsinchu, Taiwan*
Chun-Yao Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*

121.35 Chameleon: A Thermally Adaptive Error Correction Code Design for STT-MRAM LLCs
Bi Wu, Beibei Zhang, **Yuanqing Cheng** - *Beihang Univ., Beijing, China*
Ying Wang - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*
Dijun Liu - *Beihang Univ., Beijing, China*
Aida Todri-Sanial - *Centre National de la Recherche Scientifique, Montpellier, France*
Weisheng ZHAO - *Beihang Univ., Beijing, China*

121.36 Hardware-Accelerated Secured Náve Bayesian Filter Based on Partially Homomorphic Encryption
Song Bian, Masayuki Hiromoto, Takashi Sato - *Kyoto Univ., Kyoto, Japan*

121.37 ASP: A Fast Adversarial Attack Example Generation Framework Based on Adversarial Saliency Prediction.
Fuxun Yu, Qide Dong, Xiang Chen - *George Mason Univ., Fairfax, VA*

121.38 Improving I/O Performance of Large-Page Flash Storage Systems Using Subpage-Parallel Reads
Jisung Park, Myungsuk Kim, Youngsun Song - *Seoul National Univ., Seoul, Republic of Korea*
Sungjin Lee - *Daegu Gyeongbuk Institute of Science and Technology, Daegu, Republic of Korea*
Jihong Kim - *Seoul National Univ., Seoul, Republic of Korea*

121.39 Multilayer Photonic Reservoir Computing for Large-Scale Information Processing
Dharanidhar Dang - *Texas A&M Univ., College Station, TX*
Karthik Swaminathan - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Syed Ali Hasnain, Rabi N. Mahapatra - *Texas A&M Univ., College Station, TX*

WORK-IN-PROGRESS POSTER SESSION

121.40 DiReCt: Resource-Aware Dynamic Model Reconfiguration for Convolutional Neural Network in Mobile Systems
Zirui Xu, Zhuwei Qin, Fuxun Yu, Xiang Chen - *George Mason Univ., Fairfax, VA*

121.41 Methodology Support and Evaluation for Precise Timing Spiking Computation Architectures
Thomas Mesquida - *Univ. Grenoble Alpes & CEA-LETI Minatec, Grenoble, France*
Alexandre Valentian, Dominique Morche, Gilles Sicard, Edith Beigne - *CEA-LETI Minatec, Grenoble, France*

121.42 Towards Post-quantum Enabled Wireless Sensor Networks
Johanna Sepulveda, Shiyang Liu - *Technische Univ. München, Germany*
Jose M. Bermudo Mera - *Katholieke Univ. Leuven, Belgium*

NETWORKING RECEPTION AND WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm || Room: Level 2 Lobby || Event Type: Networking
Keywords: Any

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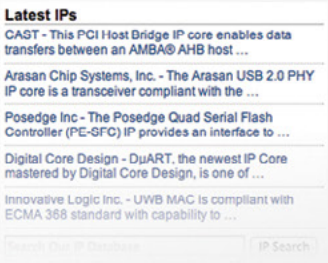

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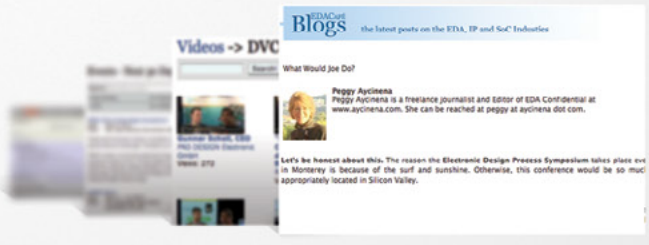

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DAC BEST PAPER AWARD PRESENTATION

Time: 9:00 - 9:20am || Room: 3008

DAC will present the Research Best Paper Award and Best Poster as well as the Designer/IP Track Best Presentation Awards.

KEYNOTE: AUTOMATION VS. AUGMENTATION: SOCIALLY ASSISTIVE ROBOTICS AND THE FUTURE OF WORK

MAJA MATARIĆ – *Professor and Chan Soon-Shiong Chair of Computer Science, Neuroscience, and Pediatrics, Univ. of Southern California, Los Angeles, CA*

Time: 9:20 - 10:00am || Room: 3008 || Keywords: Any Topic Area: Machine Learning/AI

Robotics is booming all around us. A field that was originally driven by the desire to automate physical work is now raising concerns about the future of work. Less discussed but no more important are the implications on human health, as the science on longevity and resilience indicates that having the drive to work is key for health and wellness. However, robots, machines that were originally invented to automate work, are also becoming helpful by not doing any physical work at all, but instead by motivating and coaching us to do our own work, based on evidence from neuroscience and behavioral science demonstrating that human behavior is most strongly influenced by physically embodied social agents, including robots.The field of socially assistive robotics (SAR) focuses on developing intelligent socially interactive machine that that provide assistance through social rather than physical means. The robot's physical embodiment is at the heart of SAR's effectiveness, as it leverages the inherently human tendency to engage with lifelike (but not necessarily human-like or otherwise biomimetic) agents. People readily ascribe intention, personality, and emotion to robots; SAR leverages this engagement to develop robots capable of monitoring, motivating, and sustaining user activities and improving human learning, training, performance and health outcomes. Human-robot interaction (HRI) for SAR is a growing multifaceted research field at the intersection of engineering, health sciences, neuroscience, social, and cognitive sciences, with rapidly growing commercial spinouts. This talk will describe research into embodiment, modeling and steering social dynamics, and long-term adaptation and learning for SAR, grounded in projects involving multi-modal activity data, modeling personality and engagement, formalizing social use of space and non-verbal communication, and personalizing the interaction with the user over a period of months, among others. SAR systems have been validated with a variety of user populations, including stroke patients, children with autism spectrum disorders, elderly with Alzheimer's and other forms of dementia; this talk will cover the short, middle, and long-term commercial applications of SAR, as well as the frontiers of SAR research.

Biography: Maja Matarić is Chan Soon-Shiong Professor of Computer Science, Neuroscience, and Pediatrics at the University of Southern California, founding director of the USC Robotics and Autonomous Systems Center, and Vice Dean for Research in the Viterbi School of Engineering. She received her MS and PhD from MIT in Computer Science and AI, and her BS in Computer Science from the University of Kansas. She is Fellow of AAAS, IEEE, and AAAI, and the recipient of the US Presidential Award for Excellence in Science, Mathematics and Engineering Mentoring (PAESMEM), Anita Borg Institute Women of Vision Award in Innovation, the Okawa Foundation Award, NSF Career Award, MIT TR35 Award, and IEEE RAS Early Career Award. A pioneer of distributed robotics and, more recently, socially assistive robotics, Prof. Matarić's research enables robots to help people through social interaction in therapy, rehabilitation, training, and education, developing robot-assisted therapies for autism, stroke, Alzheimer's and other special needs, as well as wellness interventions (http://robotics.usc.edu/interaction/). She has published extensively, authored the popular robotics textbook "The Robotic Primer" (MIT Press), has served as associate editor on three journals, and on the NSF CISE Advisory Committee and other advisory boards. Prof. Matarić' is actively involved in K-12 STEM outreach, having obtained federal and industry grants to develop free teacher training and open-source curricular materials for in-school and after-school robotics courses that engage student interest in science, technology, engineering, and math (STEM) topics and careers. She is also founder and CSO of Embodied, Inc. (www.embodied.me).

63 SOLID IDEAS IN SOLID STATES

Time: 10:30am - 12:00pm || Room: 3014 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies, Architecture & System Design
Topic Area: ESS, ESS

CHAIR:
Li Jiang - *Shanghai Jiao Tong Univ., Shanghai, China*

CO-CHAIR:
Swaroop Ghosh - *Pennsylvania State Univ., State College, PA*

With fast technology advances, future SSDs built with 3D flash and/or large page sizes face severe performance, reliability, and write amplification issues. This session consists of papers that address these issues: a hardware-assisted mapping mechanism is proposed to speed up the logic-to-physical page translation; a fine-grained scheduling mechanism is designed to enable one-shot programming; a new polar code scheme is developed to improve the reliability of future SSDs; and a compression-based page update scheme is proposed to minimize write amplification in large SSDs.

63.1 FMMU: A Hardware-Accelerated Flash Map Management Unit for Scalable Performance of Flash-Based SSDs
Yeong-Jae Woo - *Seoul National Univ., Seoul, Republic of Korea*
Sheayun Lee - *Kookmin Univ., Seoul, Republic of Korea*
Sang Lyul Min - *Seoul National Univ., Seoul, Republic of Korea*

63.2 Minimizing Write Amplification to Enhance Lifetime of Large-Page Flash-Memory Storage Devices
Wei-Lin Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Tseng-Yi Chen, Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., Taipei, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

63.3 Proactive Channel Adjustment to Improve Polar Code Capability for Flash Storage Devices
Kun-Cheng Hsu - *National Taiwan Univ., Taipei, Taiwan*
Che-Wei Tsao - *Academia Sinica and National Taiwan Univ., Taipei, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Tei-Wei Kuo - *National Taiwan Univ. & Academia Sinica, Taipei, Taiwan*
Yu-Ming Huang - *Macronix International Co., Ltd., Hsinchu, Taiwan*

63.4 Achieving Defect-Free Multilevel 3D Flash Memories with One-Shot Program Design
Chien-Chung Ho - *National Chung Cheng Univ. & Academia Sinica, Chiayi, Taiwan*
Yung-Chun Li - *Macronix International Co., Ltd., Hsinchu, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Yu-Ming Chang - *Macronix International Co., Ltd., Hsinchu, Taiwan*

64 ARCH NEMESIS: ARCHITECTURAL SECURITY

Time: 10:30am - 12:00pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Any || Topic Area: Security/Privacy

CHAIR:
Avinash Varna - *Intel Corp., Chandler, AZ*

Architectures are leaky; they emit information through power, time, electromagnetic emanations, and other side channels. This session describes how to use these side channels to understand the instructions being executed, determine unspecified microarchitectural features, extract the secure key from encryption code running on GPUs, and obfuscating GPU architectural features.

64.1 Power-Based Side-Channel Instruction-Level Disassembler
Jungmin Park, Xiaolin Xu, Yier Jin, Domenic Forte, Mark Tehranipoor - *Univ. of Florida, Gainesville, FL*

64.2 Side-Channel Security of Superscalar CPUs: Evaluating the Impact of Micro-Architectural Features
Alessandro Barenghi, Gerardo Pelosi - *Politecnico di Milano, Italy*

64.3 Electro-Magnetic Analysis of GPU-Based AES Implementation
Yiwen Gao, Hailong Zhang, Wei Cheng, Yongbin Zhou, Yuchen Cao - *Chinese Academy of Sciences & Institute of Information Engineering, Chinese Academy of Sciences, Beijing, China*

64.4 GPU Obfuscation: Attack and Defense Strategies
Abhishek Chakraborty, Yang Xie, Ankur Srivastava - *Univ. of Maryland, College Park, MD*

65 ADVANCING EMBEDDED SOFTWARE BEYOND FUNCTIONALITY

Time: 10:30am - 12:00pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Architecture & System Design || Topic Area: ESS

CHAIR:
Gunar Schirner - *Northeastern Univ., Boston, MA*

CO-CHAIR:
Eugenio Villar - *Univ. of Cantabria, Santander, Spain*

Next to correct functionality, embedded software design for heterogeneous multi- and many-core platforms must satisfy non-functional properties such as real-time behavior, energy efficiency, and power consumption.

This session presents four papers on embedded software analysis and optimization methods covering accelerators, caches, and mobile displays. The first paper presents a measurement-based WCET analysis considering cache behavior. Schedulability and response-time analysis for heterogeneous multi-core platforms are covered in the next two contributions. The fourth paper addresses energy efficiency by co-managing the system together with the display resolution.

65.1 Measurement-Based Cache Representativeness on Multipath Programs
Suzana Milutinovic, Jaume Abella, Enrico Mezzetti, Francisco J. Cazorla - *Barcelona Supercomputing Center & IIIA-CSIC, Barcelona, Spain*

65.2 Resource-Aware Partitioned Scheduling for Heterogeneous Multicore Real-Time Systems
Jianjun Han, Wen Cai - *Huazhong Univ. of Science & Technology, Wuhan, China*
Dakai Zhu - *Univ. of Texas at San Antonio, TX*

65.3 Response-Time Analysis of DAG Tasks Supporting Heterogeneous Computing
Maria A. Serrano, Eduardo Quiñones - *Barcelona Supercomputing Center, Barcelona, Spain*

65.4 Duet: An OLED & GPU Co-Management Scheme for Dynamic Resolution Adaptation
Han-Yi Lin, Chia-Chun Hung - *National Taiwan Univ., Taipei, Taiwan*
Pi-Cheng Hsiu - *Academia Sinica, Taipei, Taiwan*
Tei-Wei Kuo - *National Taiwan Univ. & Academia Sinica, Taipei, Taiwan*

66 SPECIAL SESSION: I-C-U: ADVANCES IN INTEGRATED CIRCUIT REVERSE ENGINEERING AND PHYSICAL ATTACKS

Time: 10:30am - 12:00pm || Room: 3020 || Event Type: Special Session
Keywords: Any || Topic Area: Security/Privacy, EDA

CHAIR:
Amir Khatib Zadeh - *Intel Corp., Portland, OR*

ORGANIZER:
Domenic Forte - *Univ. of Florida, Gainesville, FL*

Integrated circuit (IC) reverse engineering provides both a reassurance and concern for industry, government, and modern society. Globalization of the semiconductor industry has resulted in well-documented concerns such as counterfeiting, piracy, and hardware Trojan insertion. For such instances, reverse engineering represents an important tool for validating the performance, quality, authenticity, and integrity of electronics. On the other hand, reverse engineering can be responsible for as many threats as solutions. However, regardless of the goal, it is more important to understand how it is performed and its challenges. The primary goal of this session is to address the myths surrounding IC reverse engineering and invasive physical attacks – that they are too time consuming and expensive to execute for all but nation states. In the three talks of this special session, the speakers will provide concrete samples/evidence of what they've reverse engineered/attacked and how simple these processes are becoming.

66.1 Large Scale Integrated Circuit Reverse Engineering Below 14 nm. Motivation, Challenges, and Opportunities
Chris Pawlowicz - *TechInSights, Ontario, Canada*

66.2 Fully Automated Plasma FIB IC Deprocessing and Reverse Engineering
Edward Principe - *Synchrotron Research, Inc., Melbourne Beach, FL*
Navid Asadi - *Univ. of Florida, Gainesville, FL*
Michael DiBattista - *Varioscale, Inc., San Marcos, CA*
Nicolas Piche - *Object Research Systems, Montreal, Canada*

66.3 Semi-invasive Physical Attacks from IC Backside and Possible Countermeasures
Shahin Tajik, Jean-Pierre Seifert, Christian Boit - *Technische Univ. Berlin, Germany*

67 THE ART OF MAPPING FOR ACCELERATORS

Time: 10:30am - 12:00pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Architecture & System Design || Topic Area: EDA

CHAIR:
Jiang Hu - *Texas A&M Univ., College Station, TX*

CO-CHAIR:
Sri Parameswaran - *Univ. of New South Wales, Sidney, Australia*

Application mapping is critical to the success of coarse-grained reconfigurable arrays (CGRAs) and accelerator-rich architectures. The first three papers of this session present advances in mapping for CGRAs: a resource-aware mapping scheme, an exhaustive architecture-agnostic mapping method, and a technique for scheduling and mapping of deeply nested loops. The last paper explores an automatic strategy to optimize the design of accelerator memory hierarchies.

67.1 RAMP: Resource-Aware Mapping for CGRAs
Shail Dave, Mahesh Balasubramanian - *Arizona State Univ., Tempe, AZ*
Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*

67.2 An Architecture-Agnostic Integer Linear Programming Approach to CGRA Mapping
S. Alexander Chin, Jason H. Anderson - *Univ. of Toronto, Canada*

67.3 DNestMap: Mapping Deeply-Nested Loops on Ultra-Low Power CGRAs
Manupa Karunaratne, Cheng Tan, Aditi Kulkarni Mohite, Tulika Mitra, Li-Shiuan Peh - *National Univ. of Singapore, Singapore*

67.4 Locality-Aware Memory Assignment and Tiling
Samuel Rogers, Hamed Tabkhi - *Univ. of North Carolina, Charlotte, NC*

68 ENHANCING MANUFACTURABILITY AND RELIABILITY IN ADVANCED TECHNOLOGY NODES

Time: 10:30am - 12:00pm || Room: 3024 || Event Type: Research Reviewed
Keywords: Physical Design & DFM || Topic Area: EDA

CHAIR:
Charles Chiang - *Synopsys, Inc., Mountain View, CA*

CO-CHAIR:
Evangeline F.Y. Young - *Chinese Univ. of Hong Kong, Hong Kong, China*

This session presents assessments and new analysis techniques for yield, reliability and mask optimisations for advanced technology nodes. The first paper uses a GAN neural network to accelerate mask optimization. The second paper presents a Bayesian model for dimensionality reduction for fast estimation of SRAM failure regions. The third paper proposes compact models for interconnect aging including electromigration, thermomigration and stress migration. The last paper presents a sampling methodology for searching failure regions with reduced sample size and better efficiency and accuracy.

68.1 GAN-OPC: Mask Optimization with Lithography-Guided Generative Adversarial Nets
Haoyu Yang - *Chinese Univ. of Hong Kong, Shatin,, Hong Kong*
Shuhe Li, Yuzhe Ma, Bei Yu, Evangeline Young - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*

68.2 An Efficient Bayesian Yield Estimation Method for High Dimensional and High Sigma SRAM Circuits
Jinyuan Zhai, **Changhao Yan** - *Fudan Univ., Shanghai, China*
Sheng-Guo Wang - *Univ. of North Carolina, Charlotte, NC*
Dian Zhou - *Fudan Univ. & Univ. of Texas at Dallas, Dallas, TX*

68.3 RAIN: A Tool for Reliability Assessment of Interconnect Networksâ€"Physics to Software
Ali Abbasinasab, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

68.4 A Fast and Robust Failure Analysis of Memory Circuits Using Adaptive Importance Sampling Method
Xiao Shi - *Univ. of California, Los Angeles & Fudan Univ., CA*
Fengyuan Liu, Yang Jun - *Southeast Univ., Nanjing, China*
Lei He - *Univ. of California, Los Angeles, CA*

69 BUILDING FAST AND EFFICIENT NEURAL NETWORKS

Time: 1:30pm - 3:00pm || Room: 3014 || Event Type: Research Reviewed
Keywords: Architecture & System Design || Topic Area: Machine Learning/AI, Design

CHAIR:
Michael Huebner - *Ruhr Univ. Bochum, Germany*

CO-CHAIR:
Swagath Venkataramani - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

This session includes papers that present innovative solutions to improve efficiency and performance of neural networks. The first two papers present efficient implementations of the Winograd convolutional neural network (CNN) algorithm. The first paper proposes a sparse-optimized dataflow and a load-balancing algorithm for enhancing CNN efficiency. The second paper focuses on an efficient implementation targeting IoT edge devices. The third paper discusses a kernel transformation method to reduce computations and improve performance and power efficiency of binary- and ternary-weight neural networks. The fourth paper pursues mapping XNOR and bitcount operations in binary neural networks onto content addressable memory (CAM) arrays.

69.1 SpWA: An Efficient Sparse Winograd Convolutional Neural Networks Accelerator on FPGAs
Liqiang Lu, Yun Liang - *Peking Univ., Beijing, China*

69.2 Efficient Winograd-Based Convolution Kernel Implementation on Edge Devices
Athanasios Xygkis - *Intel Corp. & National Technical Univ. of Athens, Leixlip, Ireland*
Lazaros Papadopoulos - *National Technical Univ. of Athens, Athens, Greece*
David M. Moloney - *Intel Corp., Leixlip, Ireland*
Dimitrios Soudris - *National Technical Univ. of Athens, Athens, Greece*
Sofiane Yous - *Intel Corp., Leixlip, Ireland*

69.3 An Efficient Kernel Transformation Architecture for Binary- and Ternary-Weight Neural Network Inference
Shixuan Zheng - *Tsinghua Univ., Beijing, China, China*
Shouyi Yin - *Tsinghua Univ., Beijing, China*
Yonggang Liu - *Tsinghua Univ., Beijing, China, China*
Leibo Liu - *Tsinghua Univ., Beijing, China*
Shaojun Wei - *Tsinghua Univ., Beijing, China, China*

69.4 Content Addressable Memory Based Binarized Neural Network Accelerator Using Time-Domain Signal Processing
Woong Choi, **Kwanghyo Jeong**, Kyungrak Choi, Kyeongho Lee, Jongsun Park - *Korea Univ., Seoul, Republic of Korea*

70 WHY AND HOW TO SECURE YOUR DESIGN

Time: 1:30 - 3:00pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Any || Topic Area: Security/Privacy

CHAIR:
Francesco Regazzoni - *ALaRI, Lugano, Switzerland*

CO-CHAIR:
Helena Handschuh - *Rambus Cryptography Research Devision, San Francisco, CA*

Security is an increasingly important design constraint, but one that is often nebulous and always difficult to get correct. This session describes techniques aimed to mitigate this confusion with the goal of creating secure FPGAs, using 3D manufacturing to enhance the chip security, and understanding the effectiveness of fault attacks on a soft processor.

70.1 A Security Vulnerability Analysis of SoCFPGA Architectures
Sumanta Chaudhuri - *Télécom ParisTech & Univ. Paris-Saclay, Paris, France*

70.2 Raise Your Game for Split Manufacturing: Restoring the True Functionality Through BEOL
Satwik Patnaik - *New York Univ., Abu Dhabi, United Arab Emirates*
Mohammed Ashraf, Johann Knechtel, Ozgur Sinanoglu - *New York Univ., Abu Dhabi, United Arab Emirates*

70.3 Analysis of Security of Split Manufacturing Using Machine Learning
Boyu Zhang, Jonathon Magana, Azadeh Davoodi - *Univ. of Wisconsin, Madison, WI*

70.4 Inducing Local Timing Fault Through EM Injection
Marjan Ghodrati, Bilgiday Yuce, Surabhi Gujar, Chinmay Deshpande, **Leyla Nazhandali**, Patrick Schaumont - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

71 ANALYSIS AND RUNTIME SUPPORT FOR CYBER-PHYSICAL SYSTEMS

Time: 1:30 - 3:00pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Architecture & System Design, Low-Power & Reliability
Topic Area: Design, IoT

CHAIR:
Chang Wanli - *Singapore Institute of Technology, Singapore*

CO-CHAIR:
Vijay Raghunathan - *Purdue Univ., West Lafayette, IN*

Cyber-physical systems (CPS) are complex systems that interact with the physical world by leveraging the intelligence and computing power of the cloud. Functional correctness is critical as errors can lead to disastrous consequences. The first paper is an analysis tool for extracting and validating implicit assumptions in medical CPS. The second paper proposes runtime support for timing monitoring in CPS. The third paper describes a runtime structure for operating an SoC at the minimum energy point using models constructed by machine-learning. Finally, the fourth paper presents a case study on edge-cloud collaborative processing for a surveillance application.

71.1 Identifying Implicit Assumptions to Facilitate Validation in Medical Cyber-Physical System
Zhicheng Fu, Zhao Wang, Chunhui Guo, Zhenyu Zhang, Shangping Ren - *Illinois Institute of Technology, Chicago, IL*
Lui Sha - *Univ. of Illinois at Urbana-Champaign, IL*

71.2 TMA: An Efficient Timestamp-BasedMonitoring Approach to Test Timing Constraints of Cyber-Physical Systems
Mohammadreza Mehrabian, Mohammad Khayatian, Ahmed Mousa - *Arizona State Univ., Tempe, AZ*
Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*
Ya-Shian Li-Baboud - *National Institute of Standards and Technology, Gaithersburg, MD*
Patricia Derler - *National Instruments Corp., Berkeley, California*
Edward Griffor - *National Institute of Standards and Technology, Gaithersburg, MD*
Hugo A. Andrade - *Xilinx Inc. & Univ. of Texas at Austin, Berkeley, CA*
Marc Weiss - *National Institute of Standards and Technology, Boulder, CO*
John Eidson - *Univ. of California, Berkeley, CA*
Dhananjay Anand - *National Institute of Standards and Technology, Gaithersburg, MD*

71.3 Runtime Adjustment of IoT SoCs for Minimum Energy Operation
Mohammad Saber Golanbari, Mehdi B. Tahoori - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

71.4 Edge-Cloud Collaborative Processing for Intelligent Internet of Things: A Case Study on Smart Surveillance
Burhan A. Mudassar, Jong Hwan Ko, Saibal Mukhopadhyay - *Georgia Institute of Technology, Atlanta, GA*

72 SPECIAL SESSION: CO-DESIGN OF DEEP NEURAL NETS AND NEURAL NET ACCELERATORS

Time: 1:30 - 3:00pm || Room: 3020 || Event Type: Special Session
Keywords: Architecture & System Design, Emerging Architectures & Technologies, Any
Topic Area: Machine Learning/AI, ESS

CHAIR:
Doug Wightman - *Groq, Palo Alto, CA*

ORGANIZER:
Chris Rowen - *Cognite Ventures, Santa Cruz, CA*

As deep neural nets are at the core of many applications, a new problem of HW/SW co-design emerges. It is now common that even highly regarded DNN accelerators benchmark themselves on tiny datasets and antiquated DNN architectures. At the same time, for designers of novel DNN models, details on processor power-consumption and timing-models have never been harder to obtain. As a result, many DNN accelerator architects are focusing on increasing the speed on energy efficiency of older DNN models running on out of date benchmarks, and the novel DNN models, of many computer vision researchers, that increase accuracy on their target benchmarks, are only later discovered to be poorly suited to current generations of processor and DNN accelerator architectures. In this session we bring together three research groups which aim to closely coordinate the novel design of DNN models with the design of processors for efficiently executing them.

72.1 Co-designing for AI: Thinking About Deep Learning at the Systems Level
Amir Khosrowshahi - *Intel Corp., Santa Clara, CA*

72.2 Bandwidth-Efficient Deep Learning
Song Han - *Massachusetts Institute of Technology, Cambridge, MA*
William Dally - *Stanford Univ., NVIDIA, Stanford, CA*

72.3 Co-Design of Deep Neural Nets and Neural Net Accelerators for Embedded Vision Applications
Alon Amid, Amir Gholami, Kiseok Kwon, Bichen Wu, Krste Asanovic, **Kurt Keutzer** - *Univ. of California, Berkeley, CA*

73 MATHEMATICAL ATTACKS ON PLACEMENT AND ROUTING

Time: 1:30 - 3:00pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Physical Design & DFM, Interconnects, Emerging Architectures & Technologies || Topic Area: EDA

CHAIR:
Joseph Shinnerl - *Mentor, A Siemens Business, Fremont, CA*

CO-CHAIR:
Rickard Ewetz - *Univ. of Central Florida, Orlando, FL*

Complex placement and routing problems in nanometer technology nodes require advanced mathematical techniques to ensure that performance requirements and fabrication constraints are satisfied. In this session, Lagrangian relaxation, Hamiltonian cycles, linear programming, and spectral techniques are used to tackle these challenging physical design problems.

73.1 Generalized Augmented Lagrangian and Its Applications to VLSI Global Placement
Ziran Zhu, **Jianli Chen**, Zheng Peng, Wenxing Zhu - *Fuzhou Univ., Fuzhou, China*
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

73.2 Routability-Driven and Fence-Aware Legalization for Mixed-Cell-Height Circuits
Haocheng Li - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*
Wing-Kai Chow - *Cadence Design Systems, Inc. & Chinese Univ. of Hong Kong, Austin, TX*
Gengjie CHEN - *Chinese Univ. of Hong Kong, Hong Kong*
Evangeline Young, Bei Yu - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*

73.3 PlanarONoC: Concurrent Placement and Routing Considering Crossing Minimization for Optical Networks-on-Chip
Yu-Kai Chuang - *National Taiwan Univ. of Science and Technology, Kaohsiung, Taiwan*
Kuan-Jung Chen, Kun-Lin Lin, Shao-Yun Fang - *National Taiwan Univ. of Science and Technology, Taipei, Taiwan*
Bing Li, Ulf Schlichtmann - *Technische Univ. München, Germany*

73.4 Similarity-Aware Spectral Sparsification by Edge Filtering
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

74 FASTER, HIGHER, ...SAFER HLS

Time: 1:30 - 3:00pm || Room: 3024 || Event Type: Research Reviewed
Keywords: Logic & High-Level Synthesis || Topic Area: EDA

CHAIR:
Felice Balarin - *Cadence Design Systems, Inc., San Jose, CA*

CO-CHAIR:
Heinz Riener - *École Polytechnique Fédérale de Lausanne, Switzerland*

The papers in this session innovate high-level synthesis in various directions. The first two papers improve design space exploration through design templates and innovative design frameworks; the third improves design security by making the IPs harder to reverse engineer. The last paper proposes an interesting graph-coloring approach to memory partitioning.

74.1 S2FA: An Accelerator Automation Framework for Heterogeneous Computing in Datacenters
Cody Hao Yu, Peng Wei - *Univ. of California, Los Angeles, CA*
Max Grossman - *Rice Univ., Houston, TX*
Peng Zhang - *Falcon Computing Solutions, Inc., Los Angeles, CA*
Vivek Sarkar - *Georgia Institute of Technology, Atlanta, GA*
Jason Cong - *Univ. of California, Los Angeles & Falcon Computing Solutions, Inc., CA*

74.2 Automated Accelerator Generation and Optimization with Composable, Parallel and Pipeline Architecture
Jason Cong, **Peng Wei**, Cody Hao Yu - *Univ. of California, Los Angeles & Falcon Computing Solutions, Inc., CA*
Peng Zhang - Falcon Computing Solutions, Inc., Los Angeles, CA

74.3 TAO: Techniques for Algorithm-Level Obfuscation During High-Level Synthesis
Christian Pilato, Francesco Regazzoni - *Univ, of Lugano, Advanced Learning and Research Institute, Lugano, Switzerland*
Ramesh Karri - *New York Univ., Brooklyn, NY*
Siddharth Garg - *New York Univ., New York, NY*

74.4 Parallelizing Non-Stencil Memory Accesses Through Coloring Weighted Conflict Graphs
Mingjie Lin, Juan Escobedo - *Univ. of Central Florida, Orlando, FL*

75 APPROXIMATE COMPUTING: GOOD ENOUGH IS ENOUGH

Time: 3:30 - 5:30pm || Room: 3014 || Event Type: Research Reviewed
Keywords: Architecture & System Design || Topic Area: Design

CHAIR:
Matthew Guthaus - *Univ. of California, Santa Cruz, CA*

CO-CHAIR:
Shouyi Yin - *Tsinghua Univ., Beijing, China*

Low energy, small area, and high performance can be achieved by employing approximate computing. This session covers the broad range of approximate computing with first three papers on individual high-efficiency approximate adder and multiplier designs to automated optimization strategies for libraries of approximate components that limit the accuracy loss while maximizing efficiency and providing quality guarantees. The next two papers target the emerging area of approximate computing on reconfigurable fabrics, targeting FPGAs and novel coarse-grained reconfigurable architectures with hardened approximate functional units. The final paper focuses on design space exploration to examine the combined impact of multiple approximate units on the output quality.

75.1 SMApproxLib: Library of FPGA-Based Approximate Multipliers
Salim Ullah - *Technische Univ. Dresden, Dresden, Germany*
Sanjeev S. Murthy - *BITS Pilani & Technische Univ. Dresden, Goa, India*
Akash Kumar - *Technische Univ. Dresden, Dresden, Germany*

75.2 Sign-Magnitude SC: Getting 10X Accuracy for Free in Stochastic Computing for Deep Neural Networks
Aidyn Zhakatayev, Sugil Lee, Hyeonuk Sim, Jongeun Lee - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*

75.3 Area-Optimized Low-Latency Approximate Multipliers for FPGA-Based Hardware Accelerators
Salim Ullah - *Technische Univ. Dresden, Dresden, Germany*
Semeen Rehman - *Technische Univ. Wien & Technische Univ. Dresden, Vienna, Austria*
Bharath Srinivas Prabakaran - *Vienna Univ. of Technology & Technische Univ. Dresden, Wien, Austria*
Florian Kriebel, Muhammad Abdullah Hanif - *Vienna Univ. of Technology, Vienna, Austria*
Muhammad Shafique - *Technische Univ. Wien, Wien, Austria*
Akash Kumar - *Technische Univ. Dresden, Dresden, Germany*

75.4 Approximate On-the-Fly Coarse-Grained Reconfigurable Acceleration for General-Purpose Applications
Marcelo Brandalero, Luigi Carro, Antonio Carlos Schneider Beck - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
Muhammad Shafique - *Technische Univ. Wien, Wien, Austria*

75.5 LEMAX: Learning-based Energy Consumption Minimization in Approximate Computing with Quality Guarantee
Vahideh Akhlaghi, Sicun Gao, Rajesh K. Gupta - *Univ. of California, San Diego, La Jolla, CA*

76 GO WITH THE FLOW – MICROFLUIDICS, LIQUID STATE MACHINES, RESERVOIRS, AND MORE!

Time: 3:30 - 5:30pm || Room: 3016 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies || Topic Area: Design

CHAIR:
Xiang Chen - *George Mason Univ., Washington, D.C.*

CO-CHAIR:
Miao Hu - *Binghamton Univ., Binghamton, NY*

The first paper in this session presents processing in memory with SOT-MRAM. The second paper in this session discusses a new design automation tool for microfluidics. The third one discusses design-for-test techniques for continuous flow microfluidics. The fourth paper presents design techniques for neuromorphic processing with liquid state machines. The fith one proposes a novel analog reservoir computing system. The final paper exploits chaotic behavior in Mott memristors for neuromorphic computation.

76.1 PIMA-Logic: A Novel Processing-in-Memory Architecture for Highly Flexible and Energy-Efficient Logic Computation
Shaahin Angizi, Zhezhi He, Deliang Fan - *Univ. of Central Florida, Orlando, FL*

76.2 Columba S: A Scalable Co-Layout Design Automation Tool for Microfluidic Large-Scale Integration
Tsun-Ming Tseng, Mengchu Li - *Technische Univ. München & Ludwig Maximilian Univ. of Munich, Germany*
Daniel N. Freitas, Amy Mongersun, Ismail Emre Araci - *Santa Clara Univ., Santa Clara, CA*
Tsung-Yi Ho - *National Tsing Hua Univ., Hsinchu, Taiwan*
Ulf Schlichtmann - *Technische Univ. München, Germany*

76.3 Design-For-Testability for Continuous-Flow Microfluidic Biochips
Chunfeng Liu, Bing Li - *Technical University of Munich, Munich, Germany*
Tsung-Yi Ho - *National Tsing Hua Univ., Hsinchu, Taiwan*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Ulf Schlichtmann - *Technical University of Munich, Munich, Germany*

76.4 Design and Architectural Co-Optimization of Monolithic 3D Liquid State Machine-Based Neuromorphic Processor
Bon Woong Ku - *Georgia Institute of Technology, Atlanta, GA*
Yu Liu, Yingyezhe Jin - *Texas A&M Univ., College Station, TX*
Sandeep K. Samal - *Intel Corp., Hillsboro, OR*
Peng Li - *Texas A&M Univ., College Station, TX*
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

76.5 Enabling a New Era of Brain-Inspired Computing: Energy-Efficient Spiking Neural Network with Ring Topology
Kangjun Bai, Jialing Li, Kian Hamedani, **(Cindy) Yang Yi** - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

76.6 A Neuromorphic Design Using Chaotic Mott Memristor with Relaxation Oscillation
Bonan Yan, Xiong Cao, Hai Li - *Duke Univ., Durham, NC*

77 MEMORY THAT NEVER FORGETS AND MEMORY BEYOND REMEMBERING

Time: 3:30 - 5:30pm || Room: 3018 || Event Type: Research Reviewed
Keywords: Emerging Architectures & Technologies, Architecture & System Design
Topic Area: ESS, ESS

CHAIR:
Deliang Fan - *Univ. of Central Florida, Orlando, FL*

CO-CHAIR:
Cong Xu - *Hewlett-Packard Labs, Palo Alto, CA*

This session presents new architecture designs with both DRAM and non-volatile memory technologies. The first two papers describe deep neural network accelerator designs with in-DRAM computing and MLC NVM, respectively. The next two papers describe novel DRAM architectures with variable access-latency and variable refresh-latency. The next paper proposes page cache for performance improvement in NVM-based storage. The final paper presents a technique for QoS-aware scheduling in mobile platforms.

77.1 DrAcc: A DRAM Based Accelerator for Accurate CNN Inference
Quan Deng - *National Univ. of Defense Technology, Changsha, China*
Lei Jiang - *Indiana Univ., Bloomington, IN*
Youtao Zhang - *Univ. of Pittsburgh, PA*
Minxuan Zhang - *National Univ. of Defense Technology, Changsha, China*
Jun Yang - *Univ. of Pittsburgh, PA*

77.2 On-Chip Deep Neural Network Storage With Multi-Level eNVM
Marco Donato, Brandon Reagen, Lillian Pentecost, Udit Gupta, David Brooks, Gu-Yeon Wei - *Harvard Univ., Cambridge, MA*

77.3 Closed Yet Open DRAM: Achieving Low Latency and High Performance in DRAM Memory Systems
Lavanya Subramanian, Kaushik Vaidyanathan - *Intel Corp., Santa Clara, CA*
Anant Nori, Sreenivas Subramoney - *Intel Corp., Bangalore, India*
Tanay Karnik - *Intel Corp., Hillsboro, United States*
Hong Wang - *Intel Corp., Santa Clara, CA*

77.4 VRL-DRAM: Improving DRAM Performance via Variable Refresh Latency
Anup K. Das - *Drexel Univ., Philadelphia, PA*
Hasan Hassan, Onur Mutlu - *ETH Zurich, Switzerland*

77.5 Enabling Union Page Cache to Boost File Access Performance of NVRAM-Based Storage Devices
Shuo-Han Chen - *National Tsing Hua Univ., Hsinchu, Taiwan*
Tseng-Yi Chen, Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., Taipei, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

77.6 FLOSS: FLOw Sensitive Scheduling on Mobile Platforms
Haibo Zhang, Prasanna Venkatesh Rengasamy - *Pennsylvania State Univ., State College, United States*
Nachiappan Chidambaram Nachiappan - *IEEE, State College, PA*
Shulin Zhao, Anand Sivasubramaniam, Mahmut T. Kandemir, Chita R. Das - *Pennsylvania State Univ., State College, PA*

78 IS IT ABOUT TIME TO TAKE INDUCTANCE AND ELECTROMAGNETIC EFFECTS ON SOC SERIOUSLY?

Time: 3:30 - 4:25pm || Room: 3020 || Event Type: Research Panel
Keywords: Analog & Mixed-signal Design, Physical Design & DFM, Interconnects
Topic Area: EDA, Design

MODERATOR:
Yehea Ismail - *American Univ. of Cairo, Egypt*

ORGANIZER:
Magdy Abadir - *Helic, Inc., Austin, TX*

Many experts argue that increased integration of complex high speed digital, analog and RF IP blocks within SOC designs has created new opportunities for electromagnetic (EM) crosstalk that we have traditionally ignored (both inside these complex IP blocks as well as across various blocks). And that the impact of crosstalk can be further exacerbated by the decrease in signal voltage levels driven by lower-power trends in today's SOC applications. Other experts argue that internally created EM crosstalk is important in analog design but is less of an issue with today's large mixed signal SOC designs. Furthermore, RC extraction engines are doing a good job of managing this problem, as well as adding margins to tolerate the impact on timing/power is working. This panel of experts will debate the following questions: Is internally created SOC EM crosstalk a real issue today? Is inductance modeling required or not for advanced mixed-signal SOC designs? Can we continue to ignore inductance and rely on adding margins to tolerate the impact on timing, noise, etc.? And at what technology/frequency should we be worried? Do we need a sign-off methodology for EM crosstalk on all future advanced SOCs?

PANELISTS:
Ron Ho - *Intel Corp., San Jose, CA*
Vishnu Balan - *NVIDIA Corp., Santa Clara, CA*
Bari Biswas - *Synopsys, Inc., Mountain View, CA*
Yorgos Koutsoyannopoulos - *Helic, Inc., Santa Clara, CA*

79 NEW TRENDS IN EMBEDDED SYSTEMS DESIGN: LEARN, ANALYZE, AND OPTIMIZE

Time: 3:30 - 5:30pm || Room: 3022 || Event Type: Research Reviewed
Keywords: Architecture & System Design || Topic Area: ESS

CHAIR:
Seokhyeong Kang - *Pohang Univ. of Science and Technology, Pohang, Republic of Korea*

CO-CHAIR:
Oliver Bringmann - *Univ. of Tübingen, Germany*

This session deals with optimizations in multi-core architectures at the task and architectural level, as well as in wireless networks. First, a combination of design-time and run-time techniques for managing fluctuating computational workloads are presented. The second talk focuses on the determination of optimized task mappings on multi-core architectures by architecture decomposition. The session continues with a talk on fast performance simulation for neural networks on GPU architectures. Then, online learning with integrated forgetting mechanism is discussed for performance prediction of GPU/CPU architectures. Evaluating the impact of instruction set architectures on multi-core soft-error reliability is the issue of an additional talk. The last presentation focusses on optimized topology in a wireless sensor network.

79.1 Context-Aware Dataflow Adaptation Technique for Low-Power Multi-Core Embedded Systems
Hyeonseok Jung, Hoeseok Yang - *Ajou Univ., Suwon, Republic of Korea*

79.2 Architecture Decomposition in System Synthesis of Heterogeneous Many-Core Systems
Valentina Richthammer - *Ulm Univ., Ulm, Germany*
Tobias Schwarzer, Stefan Wildermann, Jürgen Teich - *Friedrich-Alexander-Univ. Erlangen-Nürnberg, Germany*
Michael GlaB - *Ulm Univ., Ulm, Germany*

79.3 NNSim: Fast Performance Estimation Based on Sampled Simulation of GPGPU Kernels for Neural Networks
Jintaek Kang, Kwanghyun Chung - *Seoul National Univ., Seoul, Republic of Korea*
Youngmin Yi - *Univ. of Seoul, Republic of Korea*
Soonhoi Ha - *Seoul National Univ., Seoul, Republic of Korea*

79.4 STAFF: Online Learning with Stabilized Adaptive Forgetting Factor and Feature Selection Algorithm
Ujjwal Gupta, Manoj Babu - *Arizona State Univ., Tempe, AZ*
Raid Ayoub, Michael Kishinevsky, Francesco Paterna - *Intel Corp., Hillsboro, OR*
Umit Y. Ogras - *Arizona State Univ., Tempe, AZ*

79.5 Extensive Evaluation of Programming Models and ISAs Impact on Multicore Soft Error Reliability
Felipe Rosa - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
Luciano Ost - *Loughborough Univ., Leicester, United Kingdom*
Vitor Bandeira, Ricardo Reis - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

79.6 Optimized Selection of Wireless Network Topologies and Components via Efficient Pruning of Feasible Paths
Dmitrii Kirov - *Univ. of Trento, Italy*
Pierluigi Nuzzo - *Univ. of Southern California, Los Angeles, CA*
Roberto Passerone - *Univ. of Trento, Italy*
Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

80 CHALLENGES & OPPORTUNITIES OF SECURE & RESILIENT PROCESSOR DESIGN: RESIST ANY MELTDOWN OF TRUST

Time: 4:30 - 5:30pm || Room: 3024 || Event Type: Research Panel
Keywords: Architecture & System Design, Any || Topic Area: Security/Privacy

MODERATOR:
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

ORGANIZERS:
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Ramesh Karri - *New York Univ., Brooklyn, NY*

Computer security has turned into a general concern in our increasingly connected and automated world. A growing demand for faster, low-power, and smarter computing platforms have produced low-power and performance optimizations. Gradually, computing systems became complex and error-prone and thereby appealing targets for attackers. This has been vividly exposed by attacks like the Heartbleed, Rowhammer, and the recent Meltdown and Spectre. Even subtle errors can have a substantial real-world impact. Until recently, even the most informed people trusted the CPUs in their platforms. While many defenses have been offered to mitigate recent attacks, the efficiency and sustainability of these solutions and their timely and correct update are challenging, raising the need for building computing structures that are more resilient against and reactive to attacks from the ground-up.This panel brings experts from industry and academia to focus on the following questions:

- How should we address the efficiency-security trade-off in current CPUs?
- How do we provide proper and timely patching?
- What are the most fundamental issues that need to be addressed and methods to be developed in designing future processors to ensure safety and security, while acting in a complex, collaborative, and heterogeneous environment?

PANELISTS:
Brian Rosenberg - *Qualcomm, Inc., San Diego, CA*
Frank McKeen - *Intel Corp., Hillsboro, OR*
Mike Hamburg - *Rambus Security Division, San Francisco, CA*
Cynthia Sturton - *Univ. of North Carolina, Chapel Hill, NC*

THURSDAY IS TRAINING DAY

TRACK 1, PART I: HOW TO BUILD VERIFICATION ENVIRONMENTS IN SYSTEMVERILOG

Time: 10:15am - 1:15pm || Room: 3000 || Event Type: Thursday is Training Day
Keywords: Test & Verification || Topic Area: EDA

This session will teach the key SystemVerilog language skills needed to understand and build constrained random verification environments, as used by UVM. The emphasis will be on learning to apply the concepts of object-oriented programming to the creation of a re-usable test bench infrastructure. Language features will be taught using working code examples, which delegates can run immediately on the EDA Playground website and will be available to use and share after the class.

Topics to be taught include the object-oriented and constrained random language features of SystemVerilog, and more particularly how to use these language features to build a verification environment that includes a component hierarchy and transaction-level communication.

The knowledge taught in this session is an essential prerequisite to the afternoon session on UVM.

This track is taught by David C. Black, Doulos Senior Member Technical Staff, who is co-author of the book, "SystemC: From the Ground Up."

SPEAKERS:

David C. Black - *Doulos Ltd., Austin, TX*

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TRACK 2, PART I: THE PYTHON LANGUAGE: BECOME A PYTHONEER!

Time: 10:15am - 1:15pm || Room: 3002 || Event Type: Thursday is Training Day
Keywords: Architecture & System Design, Any || Topic Area: EDA

This session will teach attendees the basics of the Python programming language. Python has become enormously popular as a programming language because it is compact, elegant, productive, readable, and extensible. People often remark that a Python program looks like pseudo-code, an English language description of what the code is meant to do. These attributes have led Python to be widely used as a general purpose scripting language in EDA tool flows, for scientific computing and deep learning, for embedded software test, and even for digital hardware verification and system modeling.

People sometimes become very enthusiastic about Python because of its elegance as a programming language – so-called Pythoneers. This session is your chance to become a Pythoneer, and to learn about some of the cool things you can do with Python right out-of-the-box!

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

SPEAKERS:

John Aynsley - *Doulos Ltd., Ringwood, United Kingdom*

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DOULOS

THURSDAY IS TRAINING DAY

TRACK 1, PART II: LEARN UVM USING THE EASIER UVM CODING GUIDELINES AND CODE GENERATOR

Time: 2:15 - 5:15pm || Room: 3000 || Event Type: Thursday is Training Day
Keywords: Test & Verification || Topic Area: EDA

This session will teach the basics of UVM, the Universal Verification Methodology for SystemVerilog, by taking advantage of Doulos' Easier™ UVM Coding Guidelines and Code Generator. All the main concepts of UVM will be taught using working code examples. By running the Easier™ UVM Code Generator on the EDA Playground website, delegates will be able to run UVM examples immediately, experiment with what they have learned, and share their examples with others after the class.

The session is aimed at hands-on engineers who want to start writing UVM code themselves and are looking for some specific advice on the best place to start, the right UVM features and coding idiom to use, and the pitfalls to avoid.

This track is taught by David C. Black, Doulos Senior Member Technical Staff, who is co-author of the book, "SystemC: From the Ground Up."

SPEAKERS:

David C. Black - *Doulos Ltd., Austin, TX*

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DOULOS

TRACK 2, PART II: DEEP LEARNING FOR ELECTRONIC ENGINEERS

Time: 2:15 - 5:15pm || Room: 3002 || Event Type: Thursday is Training Day
Keywords: Test & Verification || Topic Area: EDA, Machine Learning/AI

Deep learning is a very hot topic right now. Deep learning algorithms are proving effective in many existing applications such as image recognition, speech recognition, and natural language processing. Deep learning algorithms are opening the door to many totally novel applications and products, from smart homes to autonomous vehicles, from defense systems to medical systems.

Deep learning will impact DAC attendees in a number of ways, from the kinds of electronic product we design through to the algorithms used within EDA tools. The session will explain the background to deep learning, the technical jargon, and the main concepts you need to get started. Topics to be covered include basic machine learning algorithms for regression and classification, cost functions, basic neural network models, the distinction between machine learning and deep learning, the training and deployment of neural network models, an overview of the ecosystem including common deep learning software libraries and frameworks, and how to get started with deep learning. The workshop includes access to working code examples and instruction on how to run them yourself.

This session assumes a basic knowledge of Python. Attendees with no prior knowledge of Python are recommended to attend the morning session The Python Language: Become a Pythoneer!

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

SPEAKERS:

John Aynsley - *Doulos Ltd., Ringwood, United Kingdom*

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IWLS18: INTERNATIONAL WORKSHOP ON LOGIC AND SYNTHESIS

Date: Saturday, June 23 & Sunday, June 24 || Time: 8:30am - 5:00pm || Room: 3004
Event Type: Colocated Conference || Keywords: Logic & High-Level Synthesis, Emerging Architectures & Technologies, Test & Verification || Topic Area: EDA

ORGANIZERS:

Robert Wille - *Johannes Kepler Univ. Linz, Austria*
Jie-Hong Roland Jiang - *National Taiwan Univ., Taipei, Taiwan*

The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Presentations cover research on logic synthesis for both, conventional circuitry as well as emerging technologies and novel computing platforms such as nanoscale systems and biological systems. The workshop provides a platform for early dissemination of ideas and results -- highlighting important new problems in the early stages of development, without necessarily providing complete solutions. The emphasis is on novelty and intellectual rigor. Besides oral and poster presentations, keynotes and special sessions on selected topics as well as a programming contest are part of the program. Social lunches and dinner gatherings provide room for further discussions and exchanges.

THE 20TH ACM/IEEE SYSTEM LEVEL INTERCONNECT PREDICTION WORKSHOP

Date: Saturday, June 23 || Time: 9:00am - 5:00pm || Room: 3020
Event Type: Colocated Conference || Keywords: Physical Design & DFM, Interconnects, Emerging Architectures & Technologies || Topic Area: EDA

ORGANIZER:

Shiyan Hu - *Michigan Technological Univ., Houghton, MI*

The general technical scope of the workshop is the design, analysis, prediction, and optimization of interconnect and communication fabrics in electronic systems. The organizing committee invites original contributions to the workshop. These contributions include papers, tutorials, panels, special sessions, and posters. We accept papers based on novelty and contributions to the advancement of the field. The accepted papers will be published in the ACM and IEEE digital libraries.

www.SLIPonline.org

CELUG: ASSOCIATION OF HIGH PERFORMANCE COMPUTING PROFESSIONALS

Date: Tuesday, June 26 || Time: 9:00am - 5:00pm || Room: 3007
Event Type: Colocated Conference || Keywords: Any || Topic Area: EDA, IP

ORGANIZER:

Derek Magill - *Qualcomm, Inc., Austin, TX*

EDA Licensing providers, ISVs, and Enterprise Customers will come together at an event colocated with the 55th ACM/EDAC/IEEE Design Automation Conference (DAC), June 24 - 28, 2018, at the Moscone Center in San Francisco, CA. CELUG (Centralized Enterprise Licensing Users Group), the Association of High Performance Computing Professionals and the ESD Alliance are hosting this one-day event colocated at DAC 2018. This interactive event will focus on Enterprise Licensing roadmaps and private presentations, with presentations and panels addressing current and future challenges to making high technology tools and users more productive. This colocated event will bring Licensing Solution Providers and Independent Software Vendors together with Enterprise Customers from key industries for interactive, face-to-face meetings.

CELUG Centralized Enterprise Licensing User Group

ADVANCED TECHNIQUES FOR MANAGING EDA WORKLOADS

Date: Wednesday, June 27 || Time: 12:00 - 5:30pm || Room: 3007
Event Type: Colocated Conference || Keywords: Architecture & System Design
Topic Area: EDA

As complexity in semiconductors and competitiveness in the marketplace increase, so do the demands placed upon compute and storage infrastructure which plays a pivotal role in Electronic Design Automation (EDA). Massive growth of data associated with more complex designs challenges storage and workload management alike. Balancing workloads and data types puts pressure on administrators to deliver application performance and reduce bottlenecks for faster time to market. Please join IBM at this complimentary annual workshop and learn how to bring EDA designs to market faster with improved performance, manageability and ease of use. Our technical experts will show you how to improve delivery schedules by driving EDA application performance and reducing bottlenecks that waste expensive resources. You will hear directly from our developers about the latest features in IBM Spectrum™ LSF®, IBM Spectrum Scale™, while we demonstrate how you can improve operational efficiency.

Agenda:

12:00 Registration & Lunch

12:30 Welcome & What's New in Spectrum LSF?
Bill McMillan, *Global Offering Manager, IBM Spectrum Computing*

13:30 User Presentation

14:00 Is Your Fle System Slowing You Down? Choosing a High Performance File System for EDA Workloads

14:30 User Presentation: Efficient Verification at IBM, Keeping 350K Cores Fed
Leon Stok, *Vice President, Electronic Design Automation, IBM Systems*
Daniel Coops, *Functional Manager, EDA Verification Tools, IBM Systems*

15:00 Break

15:15 Using GPU's with IBM Spectrum LSF
You Bing Li, IBM Spectrum LSF Development

15:45 Running Containerised Workloads with LSF
John Welch/Larry Adams, IBM

16:15 Burning Issues / Q&A

16:30 Wrap Up & Networking Reception

Attend and you will learn how to:

- Optimize all resources including compute utilization and license management
- Maximize I/O and share data globally
- Reduce bottlenecks and maximize data transfer
- Learn from case studies from peers

CONFERECE HOST:
Bill McMillan
Global Offering Leader for the IBM Spectrum LSF family
IBM Systems - Software Defined Infrastructure

DESIGN AUTOMATION SUMMER SCHOOL

Date: Sunday, June 24 || Time: 7:30am - 6:00pm || Room: 3003 || Event Type: Additional Meeting || Keywords: Architecture & System Design || Topic Area: EDA

ORGANIZERS:

Jier Jin - *Univ. of Central Florida, Orlando, FL*
Muhammad Shafique - *Technische Univ. Wien, Vienna, Austria*
Jayita Das - *Intel Corp., Hillsboro, OR*

The Design Automation Summer School (DASS) is a one-day intensive course on research and development in design automation (DA). Each topic in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments, and indicate remaining challenges. This program is intended to introduce and outline emerging challenges, and to foster creative thinking in the next generation of EDA engineers.

The 2018 SIGDA Design Automation Summer School is co-hosted by A. Richard Newton Young Fellowship Program at DAC. All the students receiving the fellowship (excluding the mentors) are required to attend DASS event.

For additional details go to: http://www.sigda.org/dass

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A. RICHARD NEWTON YOUNG FELLOW PROGRAM WELCOME BREAKFAST & ORIENTATION

Date: Sunday, June 24 || Time: 7:30am - 9:00am || Room: 3003
Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Welcome Breakfast and Orientation
Sunday, June 24
7:30 - 9:00am
Room: 3003

Poster Presentation (Colocated with the Ph.D. Forum)
Tuesday, June 26
7:00 - 9:00pm
Level 3 Lobby

Closing Session and Award Ceremony
Thursday, June 28
6:00 - 6:45pm
Room: 3003

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HACK@DAC: FINALS

Date: Sunday, June 24 || Time: 8:00am - 5:00pm || Room: 3000
Event Type: Additional Meeting || Keywords: Architecture & System Design, Test & Verification, Contests || Topic Area: Security/Privacy, Design

ORGANIZERS:

Dan Holcomb - *Univ. of Massachusetts, Amherst, MA*
Arun Kanuparthi - *Intel Corp., Hillsboro, OR*
Hareesh Khattri - *Intel Corp., Hillsboro, OR*
Jeyavijayan Rajendran - *Texas A&M Univ., College Station, TX*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Siddharth Garg - *New York Univ., New York, NY*

System-on-a-Chip (SoC) designers use third-party intellectual property (3PIP) cores and in-house IP cores to design SoCs. Trustworthiness of such SoCs can be undermined by security bugs that are unintentionally introduced during the integration of the IPs. A security weakness, if discovered and exploited when the chips are in the field, can result in a compromise or bypass of one or more product security objectives. For example, an exploited security bug may lead to a deadlock or failure of the system, or create a backdoor through which an attacker can gain remote access to leak secrets from the system. The goal of this competition is to develop tools and methods for identifying security vulnerabilities in buggy SoCs.

In this 6-hour ordeal, the top scoring student teams from phase I of the competition will compete live to find and report security bugs from an SoC that is released to them at the start of the day. These teams mimic the role of a security research team at the SoC integrator, as try to find the security vulnerabilities and report them back to the design team quickly, so they can be addressed before the SoC goes to market. The bug submissions from the teams are scored in real time by industry experts.

ACM/IEEE EARLY CAREER WORKSHOP AT DAC

Sunday, June 24 || Time: 8:30am - 6:00pm || Room: 3014
Event Type: Additional Meeting || Keywords: Any || Topic Area: Design, EDA

ORGANIZERS:

Avrial Shrivastava - *Arizona State Univ., Tempe, AZ*
Andreas Gerstlauer - *Univ. of Texas at Austin, TX*
Shishpal S. Rawat - *IEEE Council on Electronic Design Automation, Folsom, CA*
Sherie Taylor - *Intel Corp., Chandler, AZ*

This workshop is for young and mid-career faculty and professionals in the fields related to electronic design automation (EDA). The workshop will start in the morning with an interactive session borrowing techniques from IMPROV to help you improve your soft skills (interpersonal, communication etc.) with others. This is followed by presentations and panel discussions by professionals discussing diverse topics such as navigating the various challenges to better succeed and thrive in your academic or industry job, getting your projects funded and climbing academic and technical ladders, as well as improved cooperation between industry and academia research and development. In addition, the workshop will provide rich opportunities to closely interact and network with some of the established academicians, professionals, and funding officers in EDA related fields.

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SYNOPSYS/ARM/TSMC BREAKFAST PANEL: DESIGNING WITH LEADING-EDGE PROCESS TECHNOLOGY, CPU CORES, AND TOOLS

Monday, June 25, 7:15am - 8:45am || Marriott Marquis, B2 Level, Golden Gate Ballroom
Event Type: Additional Meeting || Keywords: Emerging Architectures & Technologies, Low-Power & Reliability, Physical Design & DFM || Topic Area: EDA, Design

Faster, smaller, cooler product requirements continue to challenge designers to achieve their targets. In this breakfast panel, you will learn how TSMC, Arm, and Synopsys are working together to address these challenges to enable optimized design and accelerate design closure for Arm®-based designs on the latest TSMC process technology using the Synopsys Design Platform.

IEEE CEDA AUTHOR EDUCATION TALK: ACADEMIC PUBLISHING: MANGLED MEANS AND TATTERED ENDS IN FASCINATING TIMES

Monday, June 25, 10:30 - 11:30am || Room: 3014
Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

ORGANIZERS:

Gi-Joon Nam - *IBM Research, Yorktown Heights, NY*
Miguel Silveira - *INESC-ID/IST - TU Lisbon, Lisboa, Portugal*

Sachin Sapatnekar formulated the Promising Author Problem and cast into an optimization problem in a true blue-blood EDA researcher's fashion. This talk looks at publishing from the other end of the publication pipeline, the Punished Publisher Problem as existential absurdity of the publication enterprise. There may be lessons in this talk, though lunch is likely to have a higher value.

SPEAKER:

Rajesh Gupta - *Univ. of California, San Diego, La Jolla, CA*

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PRODUCTION-READY MACHINE LEARNING FOR EDA

Monday, June 25 || Time: 10:30 - 11:30am || Room: 3000 || Event Type: Additional Meeting || Keywords: Any || Topic Area: Machine Learning/AI, EDA

The Golden Age of machine learning is upon EDA. Over the past four years, we have seen large EDA suppliers and customers grow their internal ML teams and strategies, and ML research projects are emerging in all areas of EDA. But, we have not yet seen much of this investment convert into real production flows and work. This is because it is hard to turn research prototypes into production-ready ML tools that function correctly in the real world. This talk reviews a set of second order challenges that make it difficult to bring ML solutions to production, and discusses approaches for solving them.

SPEAKERS:

Jeff Dyck - *Mentor, A Siemens Business, Saskatoon, Canada*

SYNOPSYS LUNCH: ADVANCING CUSTOM/AMS DESIGN & VERIFICATION FOR STORAGE, HPC, AND AI APPLICATIONS

Monday, June 25 || Time: 11:30am - 1:30pm || Room: Marriott Marquis, B2 Level, Golden Gate Ballroom || Event Type: Additional Meeting || Keywords: Analog & Mixed-Signal Design, Low-Power & Reliability, Emerging Architectures & Technologies Topic Area: EDA, Design

New-age applications such as storage, high-performance computing, and AI are generating exacting demands on underlying semiconductor electronics such as Flash memory, GPUs, and application-specific processors. As a result, today's IC designers increasingly have to contend with a dual set of challenges: FinFET design complexity, and stringent performance and reliability requirements demanded by these applications. At this event, designers will share their perspectives on some of these challenges and discuss how they leverage Synopsys' Custom Design solutions to address these challenges to deliver robust AMS designs.

SYNOPSYS LUNCH: BREAKTHROUGH FUSION RTL-TO-GDSII TECHNOLOGY ENABLING INDUSTRY-BEST QOR ON ADVANCED DESIGNS

Monday, June 25 || Time: 11:30am - 1:30pm || Room: Marriott Marquis, B2 Level, Golden Gate Ballroom || Event Type: Additional Meeting || Keywords: Logic & High-Level Synthesis, Physical Design & DFM, Emerging Architectures & Technologies Topic Area: EDA, Design

Paradigm-shifting Synopsys Fusion Technology changes the RTL-to-GDSII design flow with the union of best-in-class optimization and industry-golden signoff tools. Fusion Technology enables designers to accelerate the delivery of next-generation designs using shared engines across the industry's premier digital design tools and using a unique Fusion data model for both logical and physical representation. Hear from leading customers how Synopsys Fusion Technology has redefined conventional EDA tool boundaries across synthesis, place-and-route, and signoff to address advanced-node design challenges and accelerate products to market.

ACM TODAES EDITORIAL BOARD MEETING

Monday, June 25 || Time: 12:00 - 2:00pm || Room: 3005 || Event Type: Additional Meeting || Keywords: Low-Power & Reliability || Topic Area: Design

ORGANIZER:

Annie Yu - *Univ. of Southern California, Los Angeles, CA*

Annual meeting of the ACM TODAES Editorial Board

SMARTER AND FASTER VERIFICATION IN THE ERA OF MACHINE LEARNING, AI, AND BIG DATA ANALYTICS

Monday, June 25 || Time: 12:00 - 1:30pm || Room: 3002 || Event Type: Additional Meeting || Keywords: Test & Verification, Architecture & System Design || Topic Area: Design, EDA

The core engines of functional verification - formal, simulation, emulation and FPGA based prototyping - are improving in performance, capacity and memory footprint. The next leaps in productivity will require smarter verification, utilizing advanced analytics of the data created by the core engines. What will fuel these leaps? Will it be smarter management of the engines? Will Cloud help? Common threads include data analysis of cycle quality, correlation and ranking. This panel will review the requirements for verification as Machine Learning, AI, and Big Data Analytics enter mainstream adoption and will examine what impact they will have on verification productivity.

COOLEY'S DAC TROUBLEMAKER PANEL

Monday, June 25 || Time: 3:00 - 4:00pm || Room: 3000 || Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA, Design

MODERATOR:

John Cooley - *Deepchip, Holliston, MA*

Come watch EDA vendors squirm as they answer no-holds-barred, edgy, user-submitted questions about their businesses and tools. It's an old style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

PANELISTS:

Joe Sawicki - *Mentor, A Siemens Business, Wilsonville, OR*
Anirudh Devgan - *Cadence Design Systems, Inc., Austin, TX*
Dean Drako - *IC Manage, Inc., Campbell, CA*
Prakash Narain - *Real Intent, Inc., Sunnyvale, CA*
Muhammad Faisal - *Movellus, Ann Arbor, MI*
Jim Hogan - *Vista Ventures, Louisville, CO*

SYNOPSYS PRIMETIME SIG DINNER: GOLDEN TIMING, POWER, AND RELIABILITY SIGNOFF CLOSURE

Monday, June 25 || Time: 5:45 - 9:30pm || Room: Marriott Marquis, B2 Level, Golden Gate Ballroom || Event Type: Additional Meeting || Keywords: Low-Power & Reliability || Topic Area: EDA, Design

Synopsys hosts an annual event for the PrimeTime Special Interest Group at DAC, providing an opportunity for users to stay connected with the latest developments in design analysis and signoff targeting broad application markets. We are pleased to host this PrimeTime SIG event at DAC 2018. This year, we will discuss the innovation vision in industry-leading timing, power and reliability signoff technologies to help designers work smarter and improve productivity and design quality.

SYNOPSYS/SAMSUNG FOUNDRY BREAKFAST: ENABLING OPTIMAL DESIGN WITH SAMSUNG 7NM FINFET PROCESS AND SYNOPSYS DESIGN PLATFORM

Date: Tuesday, June 26 || Time: 7:15 - 8:45am || Room: Marriott Marquis, B2 Level, Golden Gate Ballroom || Event Type: Additional Meeting || Keywords: Physical Design & DFM, Low-Power & Reliability, Emerging Architectures & Technologies Topic Area: EDA, Design

As each new process technology brings with it significant advantages as well as design challenges, Samsung Foundry and Synopsys continue to collaborate to enable design in 5nm technology and beyond. At this event, you'll learn how our efforts provide a robust foundation for designers to get the most from Samsung advanced process technologies using Synopsys' Design Platform with Fusion Technology. You'll also hear how the collaboration has accelerated a customer's real-world 7nm design success.

SYNOPSYS LUNCH: AUTOMOTIVE DRIVES THE NEXT GENERATIONOF DESIGNS

Date: Tuesday, June 26 || Time: 11:30am - 1:30pm || Room: Marriott Marquis, B2 Level, Golden Gate Ballroom || Event Type: Additional Meeting || Keywords: Analog & Mixed-signal Design, Low-Power & Reliability, Physical Design & DFM || Topic Area: Automotive, Design

Automotive design is one of the hottest growing areas in the semiconductor industry. ISO 26262 is the international standard that documents functional-safety compliance for all electronic devices in vehicles from simple to smart sensors through complex autonomous driving systems. In this session, a panel of industry experts will share their vision on how their automotive designs are driving the next generation of products.

SYNOPSYS LUNCH: SOC LEADERS VERIFY WITH SYNOPSYS

Date: Tuesday, June 26 || Time: 11:30am - 1:30pm || Room: Marriott Marquis, B2 Level, Golden Gate Ballroom || Event Type: Additional Meeting || Keywords: Test & Verification || Topic Area: EDA

Synopsys will highlight next-generation verification technologies, as well as discussions about the latest developments in the verification landscape and advanced technology trends. In addition, a panel of industry experts will share their viewpoints on what is driving SoC complexity, how their teams have achieved success, and how you can apply their insights onyour next project.

IEEE CEDA DISTINGUISHED SPEAKER LUNCHEON: ENERGY EFFICIENT NEUROMORPHIC LEARNING AND INFERENCE AT NANOSCALE

Date: Tuesday, June 26 || Time: 12:00 - 1:30pm || Room: 3003 || Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

ORGANIZER:

Gi-Joon Nam - *IEEE CEDA & IBM Research, La Jolla, CA*

Learning and adaptation are key to natural and artificial intelligence in complex and variable environments. Neural computation and communication in the brain are partitioned into the grey matter of dense local synaptic connectivity in tightly knit neuronal networks, and the white matter of sparse long-range connectivity over axonal fiber bundles across distant brain regions. This exquisite distributed multiscale organization provides inspiration to the design of scalable neuromorphic systems for deep learning and inference, with hierarchical address event-routing of neural spike events and multiscale synaptic connectivity and plasticity, and their efficient implementation in silicon low-power mixed-signal very-large-scale-integrated circuits. Advances in machine learning and system-on-chip integration have led to the development of massively parallel silicon learning machines with pervasive real-time adaptive intelligence at nanoscale that begin to approach the efficacy and resilience of biological neural systems, and already exceed the nominal energy efficiency of synaptic transmission in the mammalian brain. I will highlight examples of neuromorphic learning systems-on-chips with applications in template-based pattern recognition, vision processing, and human-computer interfaces, and outline emerging scientific directions and engineering challenges in their large-scale deployment.

Biography: Gert Cauwenberghs is Professor of Bioengineering and Co-Director of the Institute for Neural Computation at UC San Diego. He received the Ph.D. in Electrical Engineering from Caltech in 1994, and was previously Professor of Electrical and Computer Engineering at Johns Hopkins University, and Visiting Professor of Brain and Cognitive Science at MIT. His research focuses on neuromorphic engineering, adaptive intelligent systems, neuron-silicon and brain-machine interfaces, and micropower biomedical instrumentation. He is a Fellow of the Institute of Electrical and Electronic Engineers (IEEE) and the American Institute for Medical and Biological Engineering (AIMBE), and was a Francqui Fellow of the Belgian American Educational Foundation. He previously received NSF CAREER, ONR Young Investigator Program and White House PECASE awards. He served IEEE in a variety of roles including recently as Editor-in-Chief of the IEEE Transactions on Biomedical Circuits and Systems.

SPEAKER:

Gert Cauwenberghs - *Univ. of California, San Diego, La Jolla, CA*

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CEDA
IEEE Council on Electronic Design Automation

MONSTER CHIPS: SCALING DIGITAL DESIGN INTO THE NEXT DECADE

Date: Tuesday, June 26 || Time: 12:00 - 1:30pm || Room: 3002 || Event Type: Additional Meeting || Keywords: Logic & High-Level Synthesis, Physical Design & DFM, Emerging Architectures & Technologies || Topic Area: EDA, Design

Modern SoC design has already become an unwieldy compute-intensive beast with multiple bottlenecks threatening tapeout schedules. How must our semiconductor design methodology change to meet the coming wave of billion-instance chips that AI and machine learning will bring? This panel of expert designers, IP providers, and EDA tool vendors will consider the top emerging trends, their design implications, and potential solutions to overcoming these imminent challenges. Topics discussed may include AI/ML trends in HPC, mobile and automotive markets, tool scalability, EDA in the cloud, 20M instance blocks, point tools vs. integrated flows, and physical design to 7nm and below.

SYNOPSYS/GLOBALFOUNDRIES DINNER: ADDRESSING THE DESIGN CHALLENGES OF IOT WEARABLES AND AUTOMOTIVE WITH 22DFX TECHNOLOGY

Date: Tuesday, June 26 || Time: 6:15 - 8:15pm || Room: Marriott Marquis, B2 Level, Golden Gate Ballroom || Event Type: Additional Meeting || Keywords: Physical Design & DFM, Emerging Architectures & Technologies || Topic Area: EDA, Design

Attend this dinner event to hear how GLOBALFOUNDRIES' dual-roadmap processes and Synopsys' technology are providing mutual customers with tools, flows, and ecosystem enablement in both high-performance and mobile markets.

BIRDS-OF-A-FEATHER MEETINGS

Date: Tuesday, June 26 || Time: 7:00 - 8:30pm || Room: Various
Event Type: Additional Meeting || Keywords: Any

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-Of-A-Feather" (BOF).

All BOF meetings are held at the Moscone Center West, Tuesday June 26 from 7:00 - 8:30pm.

To arrange a BOF Meeting, please email Trevor Kearns at trevor@dac.com

ACM SIGDA AND IEEE CEDA PH.D. FORUM

Date: Tuesday, June 26 || Time: 7:00 - 9:00pm || Room: Level 3 Lobby
Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

ORGANIZERS:

Sudeep Pasricha - *Colorado State Univ., Ft. Collins, CO*
Hai Li - *Duke Univ., Durham, NC*
Umit Ogras - *Arizona State Univ., Tempe, AZ*

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA and IEEE CEDA for senior Ph.D. students to present and discuss their dissertation research with people in the EDA community. Participation in the forum is highly competitive with acceptance rate of around 30%. The forum is open to all members of the design automation community and is free-of-charge.

For more information, please visit the ACM SIGDA Ph.D. Forum website.

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30TH ACM SIGDA UNIVERSITY DEMONSTRATION

Date: Tuesday, June 26 || Time: 7:00 - 9:00pm || Room: Level 3 Lobby || Event Type: Additional Meeting || Keywords: Any || Topic Area: EDA

ORGANIZER:

Qi Zhu - *Univ. of California, Riverside, CA*

This year marks the 30th University Demonstration at the Design Automation Conference. UD is an opportunity for university researchers to display their results and to interact with participants at DAC. Presenters and attendees at DAC are especially encouraged to participate, but participation is open to all members of the university community. The demonstrations include new EDA tools, EDA tool applications, design projects, and instructional materials.

For decades, DAC has encouraged the contributions and participation of graduate and undergraduate students globally. For further details please visit the Students & Scholarships page.

Booth Coordinators:

Chair: Qi Zhu - *Univ. of California, Riverside, CA*
Vice Chair: Anup Kumar Das - *IMEC, Peoria, IL*
Publicity Chair: Prof. Wenchao Li, - *Boston University, Boston, MA*

DOULOS LUNCH N' LEARN: TUTORIAL: PYTHON FOR SCIENTIFIC COMPUTING AND DEEP LEARNING

Date: Wednesday, June 27 || Time: 12:00 - 1:00pm || Room: 3003 || Event Type: Additional Meeting || Keywords: Test & Verification, Any || Topic Area: EDA

As well as being a general purpose programming and scripting language, Python has become one of the most popular languages for scientific computing and more recently for deep learning. Python is everywhere, and Python is cool. Python is easy to learn and Python programs are very readable, even by people who don't know Python. There are Python libraries available for doing pretty much anything.

In this tutorial you will learn enough to start using Python as a scripting language and you will become sufficiently familiar with Python to start making sense of the emerging libraries and frameworks used for deep learning, such as TensorFlow and Keras. This tutorial will show you some of the really cool things you can do with Python right out-of-the-box!

You can learn more about the Python language and about Deep Learning in the morning and afternoon sessions on 'Thursday is Training Day'.

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DOULOS

LUNCHEON PANEL: MEETING ANALOG RELIABILITY CHALLENGES ACROSS THE PRODUCT LIFE CYCLE

Date: Wednesday, June 27 || Time: 12:00 - 1:30pm || Room: 3002
Event Type: Additional Meeting || Keywords: Analog & Mixed-signal Design, Test & Verification || Topic Area: Automotive, EDA

Creating designs to meet reliability challenges has become formidable. How reliable your design is could mean a multi-million-dollar recall or leaving a loved one stranded by the roadside. While digital design lends itself to "extremes" testing, it's more difficult on the analog/mixed-signal side. Failures can be caused by thermal overstress, device aging, or design abuse. Reliability testing cannot be a few tests during final verification. It needs to be a philosophy permeating the entire design cycle. How confident you are with your design becomes a paramount decision factor. Hear from Cadence, industry, and academic experts about their experiences and expectations for reliable designs.

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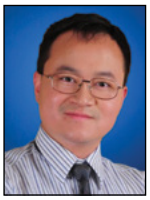

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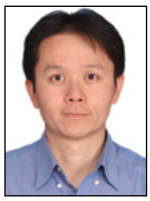

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Monday

Time	Presentation
10:30 - 11:15am	Association of HPC Pros: Intro to DIA
11:30am - 12:15pm	Si2: Si2 OpenAccess—Design Infrastructure for the Future
12:30 - 1:30pm	Microsoft / Azure: Why Cloud, Why Now?
1:30 - 2:15pm	IC Manage: 10 minutes to Hybrid Cloud Bursting – Run Existing Workflows in the Cloud without Retooling
2:30 - 3:15pm	IBM: EDA on IBM Cloud
3:30 - 4:15pm	ACM: Design for Security: A High-Level Synthesis Approach
4:30 - 5:30pm	Panel - Cloud: Cloud Computing for EDA: Pie in the Sky or Pie in the Face

Tuesday

Time	Presentation
10:30 - 11:15am	Metrics.ca: Verification 3.0 – Enabling Innovation via the Cloud
11:30am - 12:15pm	Altair: Cloud for Cloud Skeptics
12:30 - 1:30pm	Cadence - EDA on the Cloud: Are We Ready?
1:30 - 2:15pm	Google: Moving EDA to the Cloud – a Google-on-Google story
2:30 - 3:15pm	Univa: Towards a Strategic Deployment Pattern for the EDA Hybrid Cloud
3:30 - 4:15pm	AWS: Innovation at Cloud Speed for IoT, AI, and Semiconductor Design
4:30 - 5:30pm	Six Nines: Revolutionizing Semiconductor Design Workflows With HPC In The Cloud

Wednesday

Time	Presentation
10:30 - 11:15am	Dell EMC - Peeling the Onion: How Enterprise Storage Limits Tool Performance and What You Need to Do to Fix It
11:30am - 12:15pm	Pure Storage: Faster Time to Market: Eliminate Data Bottlenecks for EDA and AI Workloads
12:30 - 1:30pm	FootPrintKu PalPilot: Influencing Design Libraries with Cloud Automation
1:30 - 2:15pm	TI: CPU Oversubscription in Compute Clouds
2:30 - 3:15pm	Ellexus: Fast, Agile and Cloud Ready: How to Make Workflows Faster and Easier to Move
3:30 - 4:15pm	Alibaba: Alibaba Eco-System Enable Your Business
4:30 - 5:30pm	SuSE

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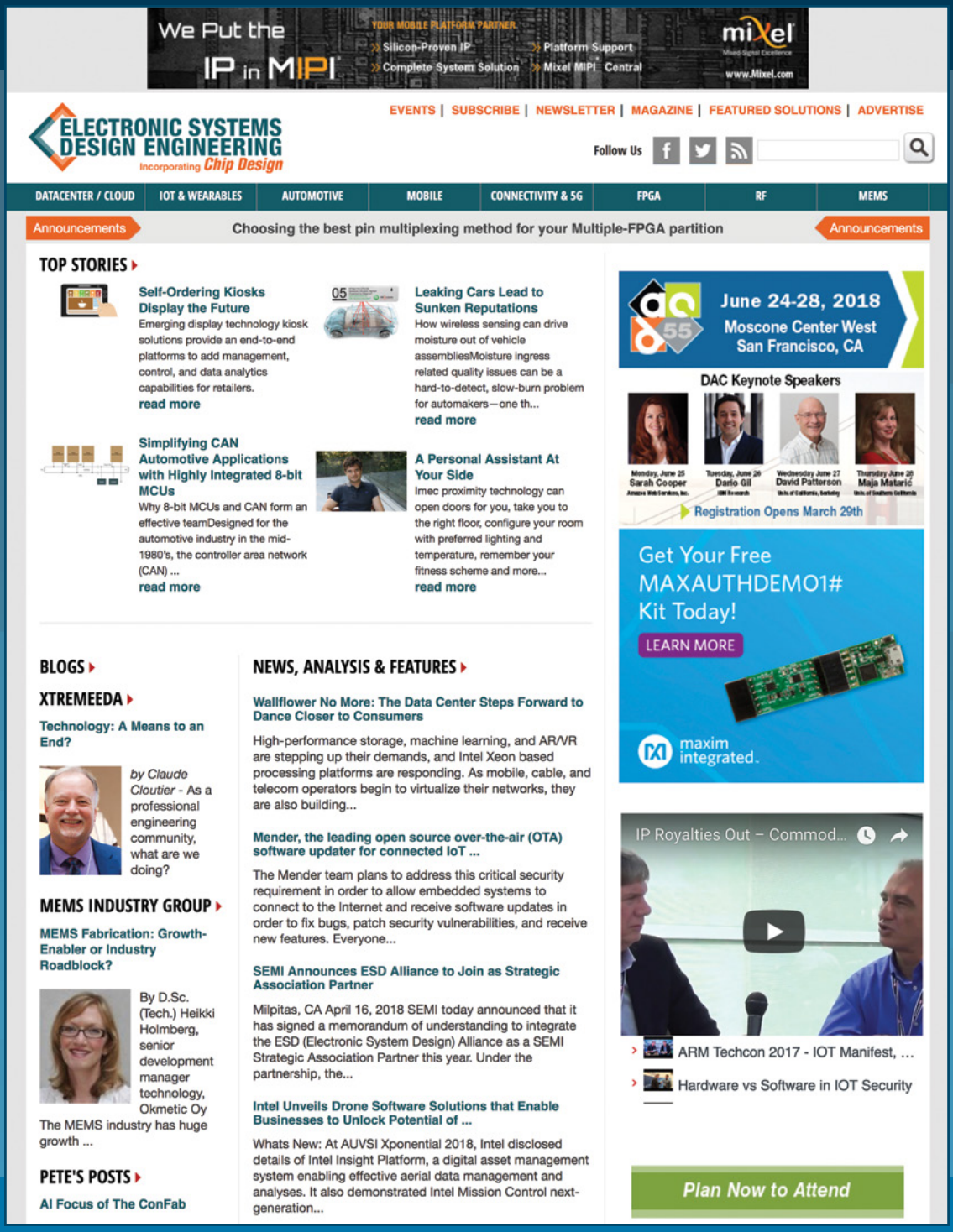

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MONDAY SPECIAL EVENT:

RTL-to-GDSII Fusion Technology Lunch at the Marriott

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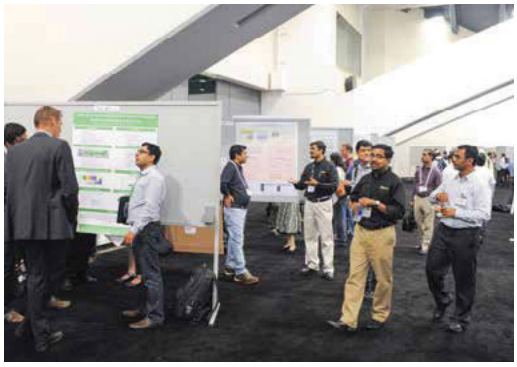

JUNE 2-6, 2019
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